Field Support Manual
Disk File Processor WDE
P4000-35
PTS6759-001



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Disk File Processor WDE
P4000-35

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SERVICE MANUAL STATUS RECORD

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1 GENERAL DESCRIPTION

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1.1 INTRODUCTION

The Disk Control Unit or Disk File Processor (DFP) is a direct memory access control unit, whose function is to locate and process a data record via one or more index levels, from a command provided by the Central Processing Unit.

The hardware-software interface is the HSI "BEZARDS". The disk CU is physical realized on one double eurocard with basic name WDE. The disk drives are connected to the control unit in a daisychain configuration.

The disk control unit allows connection of 3 5 1/4" hard disk drives with ST506 interfaces and 2 5 1/4" mini floppy disk drives with SA450 interface.
Towards the UPL-bus the control unit interfaces as a control unit with direct memory access.
Hence, the environmental required for the functioning of th disk control unit can be depicted as shown in figure 1.
Note: The maximum number of drives is drawn.

The cables representent the control- and read/write data lines.

The control unit makes use of a data buffer.

Sectors can be interleaved on a track so reading or writing a track takes a limit number of revolutions.

Error correction is used for hard disk only.

Hard disk and floppy disk actions can only be active one at the time.

The control unit will be realised on one double euro card.

The control unit is called WDE.

Following hard disk drives can be connected:

- Rodime model RO201, 202, 203, 204
- Seagate ST506/412/406
- PRIAM 506 and equivalent

Following floppy disk drives can be connected:
Philips model X3111, 3112, X3113, X3114, X3116, X3118 and Equivalent

Floppy disk drives with as well 250 as 500 kbits/s transferrate can be used; selection takes place b.m.o. straps.

It has to be noticed that for each drive configuration connected to the control unit, drives with the same access parameters have to be used.

No bad track handling is done for the floppy drives connected.

By using the 5 1/4" floppy-and 8" connection an 8" floppy drive can be connected as FD1 in the chain. see 1.4.5.3

Also 8" floppy drives with single sided, single density can be handled.

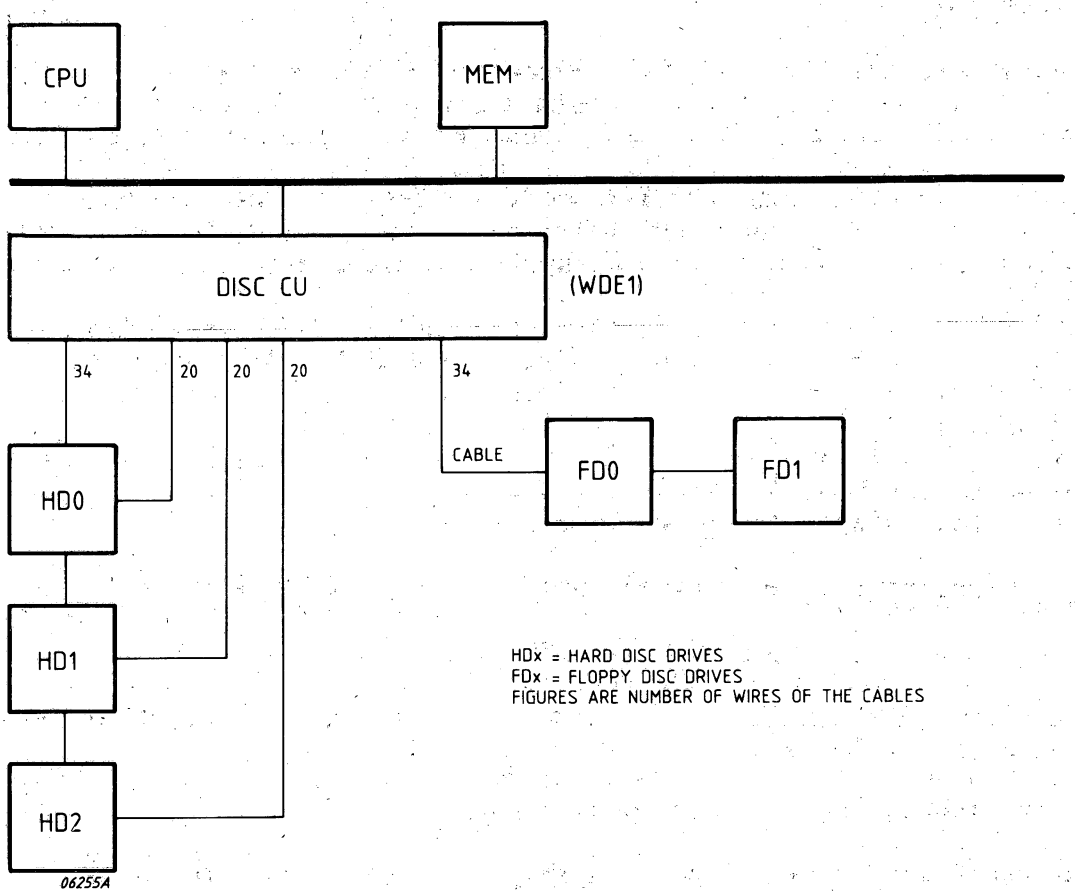

Figure 1.1 MAXIMUM CONFIGURATION

For communication with the system, two LSI chips have been designed:
The BUSLSI chip, which regulates the flow of data between the CPU, Memory and DFP, and the Interrupt Handling chip which controls interrupts in accordance with the system priority scheme.

In order to communicate with the high performance disk drives, the DFP translates HSI level commands into commands and procedures meaningful to the connected drives. It also translates status information generated by the disk drives into status information stored in the input/output descriptor at HSI Level.

1.2 PHYSICAL DESCRIPTION

The DFP has been designed on a card of the double Euro-format.

The card consists of more layers of which the inner two layers are used for power supply lines, and the outer two for the logic wiring. The allocation of the card: see concerning Field Service Manual.

1.3 TECHNICAL DATA

1.3.1 SURVEY OF DISK DRIVES

TYPE	MAN. CODE	UNFORM. CAPACITY IN OCT'S	USER CAPACITY IN OCT'S	CATALOGUE NUMBER
Hard Disk:				
Rodime	202 E	26 M	20 M	P3414
Rodime	204 E	52 M	40 M	P3416
Floppy disk:				
Philips	X3118			P3402
Philips	X3114			

1.3.2 POWER REQUIREMENTS

The power supply required by the DFP is +5V, which can be located at the connector on the system bus.

The exact voltage is given in the table below, and the equivalent circuit and waveform in Figures 1.2 and 1.3 respectively.

Voltage (V)	I max. average (A)	▷I max (A)	F max (MHz)	CO (nF)	C1 (UF)	L1 (nH)	C2 (UF)	L2 (nH)	max. rating
+5.0	3.8	0.4	3.0	3	4.0	0.1	-	-	+7V
+12.0	0.05	0.05	-	-	0.1	3	15	20	+15V
-12.0	0.03	0.03	-	-	0.1	3	15	20	-15V

load of RSLN : 0.4mA
load of clearn: 0.4mA
load of PWFN : 0.4mA
voltage tolerance +4% and -3%

In case a DTI is connected we have the following extra power load:
+5.0V: 100 mA.

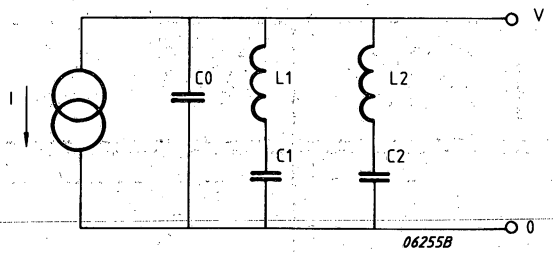

Figure 1.2 EQUIVALENT DIAGRAM

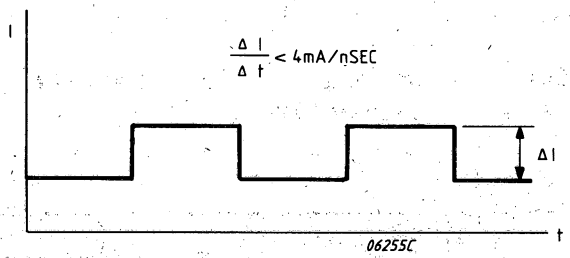

Figure 1.3 CURRENT WAVEFORM

1.3.3 PHYSICAL CHARACTERISTICS

The outside dimensions of the card used in the DFP can be seen in Figure 1.4.

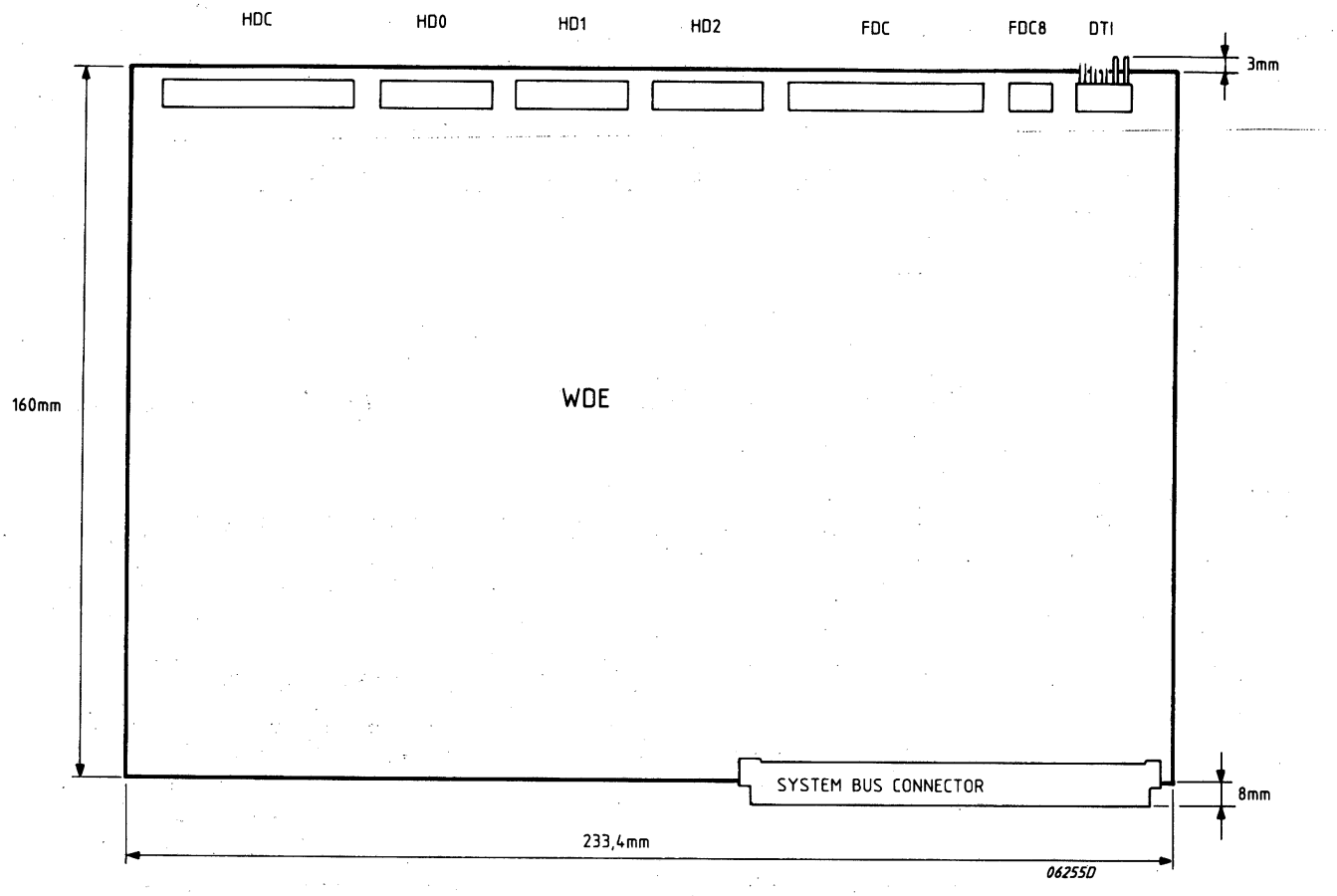

Figure 1.4 CONNECTOR LAYOUT WDE

A side view of the card showing mounted components is given in Figure 1.5. The maximum height of components (distance B) is 9mm, and the space between the cards (distance A) is 15.24mm.

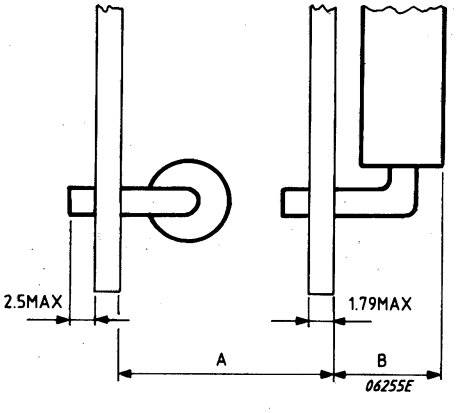

Figure 1.5 CARD, SIDE VIEW

The connector to the system interface is 96-pins male connector. In Figure 1.6 the dimensions and pin numbering are indicated.

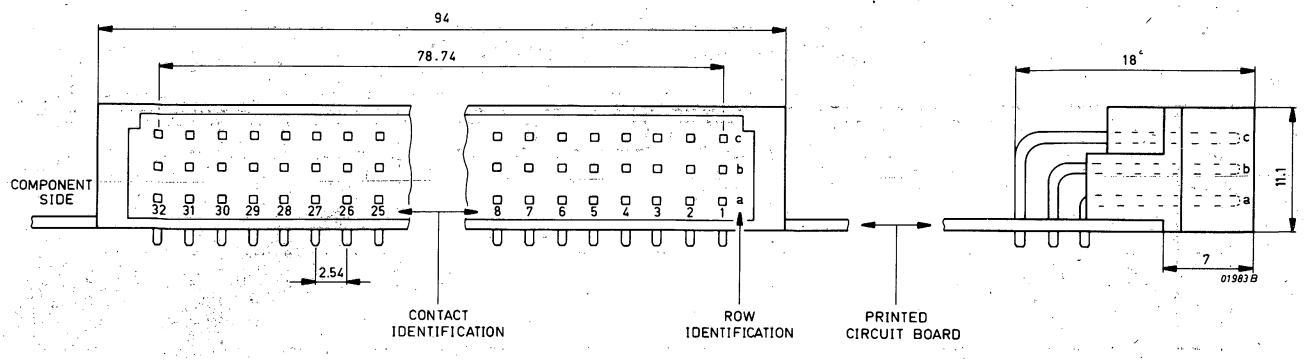

Figure 1.6 BOTTOM VIEW AND SIDE VIEW OF THE SYSTEM INTERFACE CONNECTORS

The device connectors are drawn in Figure 1.7.
There are different length of these connectors and the following list gives a summary of the lengths used for the different devices.

CONNECTOR	NO. OF PINS	LENGTH A*	LENGTH B*
HDC, FDC	34	42 mm	40.6 mm
HDO/1/2	20	24 mm	22.9 mm
FDC8	8	9 mm	7.6 mm
DTI	10	11 mm	10.2 mm

* See Figure 1.7.

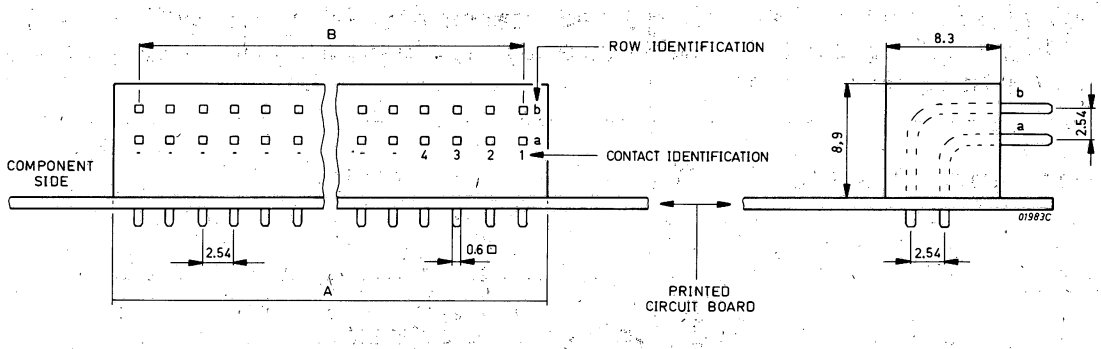

Figure 1.7 TOP VIEW AND SIDE VIEW OF DEVICE CONNECTOR

1.3.4 ENVIRONMENTAL REQUIREMENTS

1.3.4.1 CLIMATIC REQUIREMENTS

Operating Conditions:

	TEMPERATURE		REL. HUMIDITY		ABS. HUMIDITY	
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
ABSOLUTE OPERATING LIMITS	5°C	40°C	15%	90%	1,5 g/m3	25 g/m3
OPTIMUM OPERATING LIMITS	10°C	35°C	20%	80%	3 g/m3	20 g/m3

The dynamic limits T = 0.5°C / minute (no condensation).
The air velocity between the cards must be more than 1 m/sec.

Storage Conditions:
(Packed or unpacked in Ware-house)

TEMPERATURE		REL. HUMIDITY	
MIN.	MAX.	MIN .	MAX.
+3°C	+50°C	10%	90%

The dynamic limit T = 0.5°C / minute. (no condensation)

Transport Conditions:

	PACKED		UNPACKED	
	MIN.	MAX.	MIN.	MAX.
TEMPERATURE	-40°C	+70°C	-40°C	+70°C
REL. HUM. 12 HOURS	10%	100%	10%	90%
REL. HUM. 6 WEEKS	10%	98%	10%	90%
REL. HUM. 3 MONTHS	10%	90%	10%	90%

The dynamic limit T = 5°C / minute.

Air Pressure:

	MIN.	MAX.
OPERATING LIMITS	700 mbar	1100 mbar
NON-OPERATING LIMITS	450 mbar	1100 mbar

700 mbar is an altitude of approximately 2250 meters above sea-level.
450 mbar is an altitude of approximately 6300 meters above sea-level.

1.3.4.2 SHOCK AND VIBRATION REQUIREMENTS

VIBRATION REQUIREMENTS

Condition : Unpacked.
Frequency : 10 Hz to 60 Hz ; amplitude 0,2 mm.
60 Hz to 150 Hz; 3 gn.
Directions: All.

SHOCK REQUIREMENTS

Condition : Unpacked.
Requirement : Acceleration: 25 gn.
Duration: 6 ms.
(Related to half-sine pulse shape).
Directions : All.

1.3.4.3 HANDLING OF MOS-MEMORY BOARDS

Note that special care must be taken at handling, repairing or packaging of MOS (memory) modules due to static charge, which may occur and possibly discharge via one pin, so damaging or degenerating the device. It is therefore essential to prevent any difference in voltage potential to be built up between a MOS device and any surface, tool or person with which it may come into contact.
The following rules may be helpful.

a) Packing
MOS circuit boards may be packaged in a metal box, a wooden case, a cardboard box or conductive plastic, but not in ordinary plastic. These conductive or semi-conductive materials prevent from static discharge at one point.

b) Repairing
It is preferable that al work on MOS devices is carried out on a metal or conductive surface, which in some way is connected to ground-potential. All tools and the device should remain on this surface and the personnel must "discharge" themselves on it before work commences. All electrical equipment used (e.g. scope, digital voltmeters and the tip of the soldering iron) must be grounded.

c) Personnel
It is advisable for personnel to "ground" themselves before touching MOS devices, e.g. by touching a metal pipe that is grounded, or at least discharge themselves to the same potential as the working surface before commencing work.

1.4 INTERFACES

The WDE Disk File Processor has 8 interfaces.

1	The System Bus Interface	1x
3	Hard Disk Control Interface	1x
4,5,6	Hard Disk Data Interface	3x
7	Floppy Disk 5 1/4 inch Interface	1x
8	Floppy Disk 8 inch Interface	1x
9	DTI Interface	1x

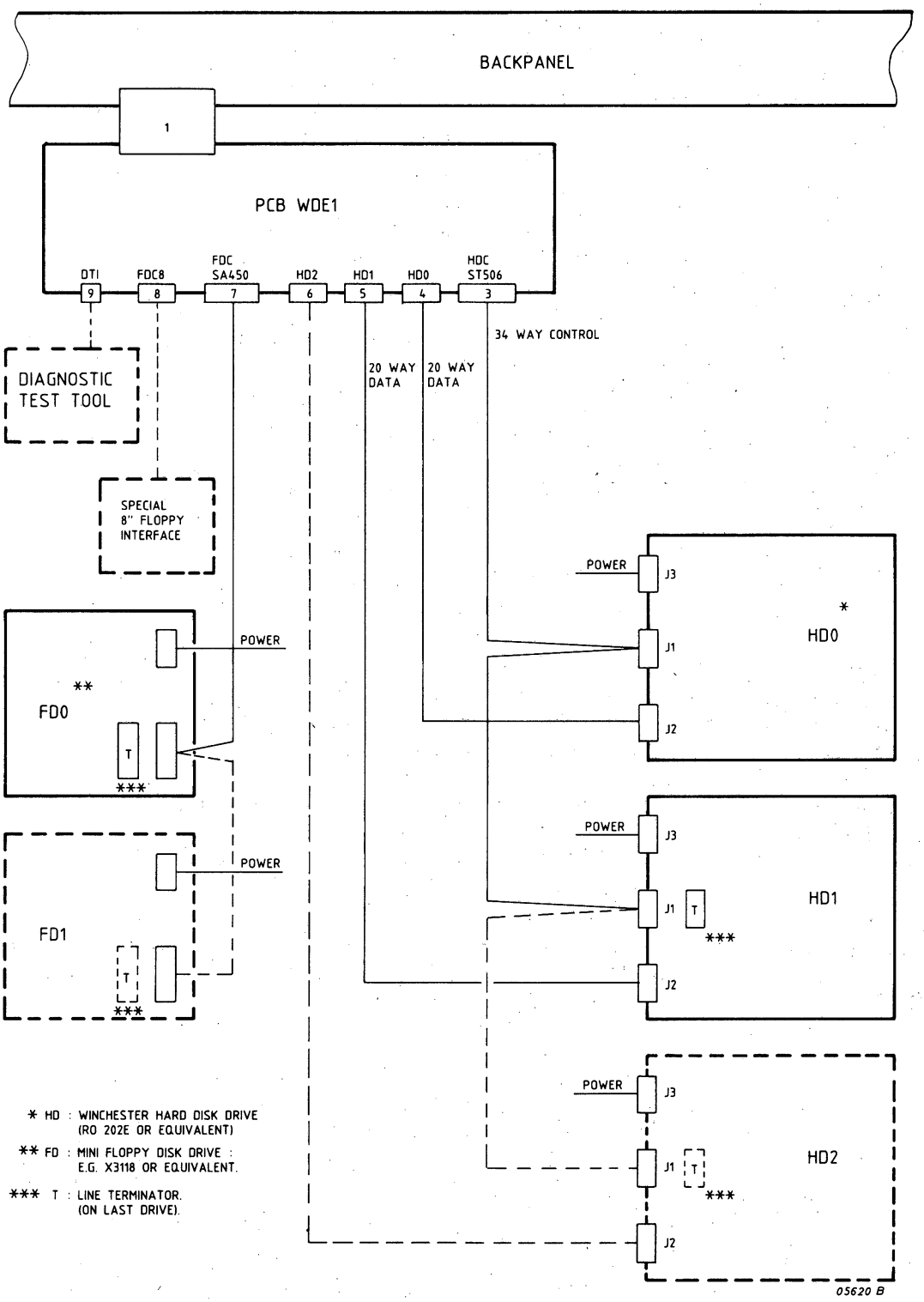

Figure 1.8 INTERFACES AND CONNECTORS

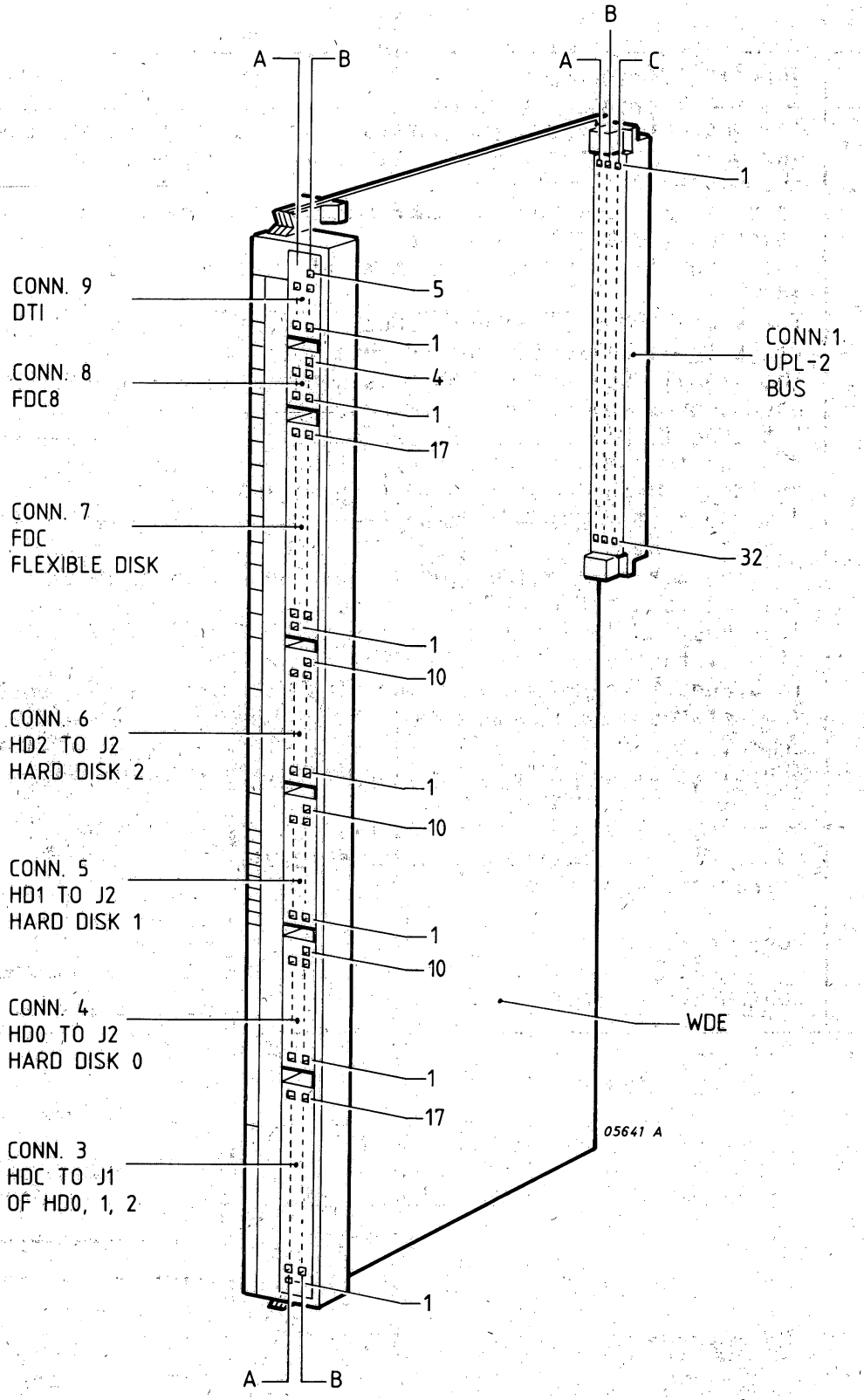

Figure 1.9 CONNECTORS WDE

1.4.1 SYSTEM BUS INTERFACES

1.4.1.1 SIGNAL DESCRIPTION

NAME	DESCRIPTION
MAD00-15	The most significant two octads of the system address bus.
MADE0-7	The most significant octad of the system address bus.
BIØ00-15	The system DATA bus.
ØKI	When OKI is received, the DFP has the possibility of being selected. ØKØ NOT generated.
ØKØ	This signal is generated if the DFP does not want to be selected.
MSN	The signal "Master Selected Not" is generated when the DFP wants to be selected and has received ØKI.
BUSRN	The signal "Bus Request Not" is set by the DFP when it wants to have control over the system bus.
TMEN	Not used in DFP.
TMPN	"Timing from Master to Peripheral Not" indicates to the DFP that the data on the bus is valid (CPU is MASTER).
TMRN	"Timing from Master to Memory Not" is an indication from the DFP that the the data on the bus is valid.
TSMN	"Timing Slave to Master Not" is an indication that the data on the bus is accepted by the slave.
BSYN	"Bus Busy Not" an indication for the DFP that the bus is occupied by the CU which has set the signal MSN.
WRITE	The signal "Write" being a zero indicates to the DFP that a send status command was received. A one indicates a CIØ-start command.
INCL	The clock signal INCL is used by the interrupt handler chip to send its interrupt address.
BCI	The Binary Coded Interrupt Address of the DFP is serially shifted out of the interrupt handler chip via this line.
CHA	Characters/Word mode.
CLEARN	
PWFN	Power Failure.
RSLN	
CUA 0-4	Control Unit number

1.4.1.2 SYSTEM BUS CONNECTOR (UPL-BUS 2)

Connector Location: F7A3

Connector Pin Assignment

PIN NUMBER	SIGNAL NAME	SIGNAL TYPE	PIN NUMBER	SIGNAL NAME	SIGNAL TYPE	PIN NUMBER	SIGNAL NAME	SIGNAL TYPE
1C01	+12VL		1B01			1A01	-12VL	
1C02			1B02	BUSRN		1A02		
1C03	BCI		1B03	MSN		1A03	INCL	
1C04	--		1B04	OV		1A04	--	
1C05	--		1B05	BSYN		1A05	--	
1C06	OV		1B06	OKO	OP*	1A06	OV	
1C07	PWFN		1B07	OKI	IP	1A07	RSLN	IP
1C08	CLEARN		1B08			1A08	ACN	OP
1C09	OV		1B09	CUAO	IP	1A09	OV	
1C10	TMPN		1B10			1A10	TSMN	OP
1C11			1B11	OV		1A11	TMRN	IP
1C12	OV		1B12	MADE0	IP	1A12	OV	
1C13	MAD00	IP*	1B13	MADE1	IP	1A13	MAD01	IP
1C14	MAD02	IP	1B14	OV		1A14	MAD03	IP
1C15	MAD04	IP	1B15	MADE2	IP	1A15	MAD05	IP
1C16	MAD06	IP	1B16	MADE3	IP	1A16	MAD07	IP
1C17	MAD08	IP	1B17	MADE4	IP	1A17	MAD09	IP
1C18	MAD10	IP	1B18	MADE5	IP	1A18	MAD11	IP
1C19	MAD12	IP	1B19	MADE6	IP	1A19	MAD13	IP
1C20	MAD14	IP	1B20	MADE7	IP	1A20	MAD15	IP
1C21	CHA	IP	1B21	OV		1A21	WRITE	IP
1C22	OV		1B22	--		1A22	OV	
1C23	BIO08N	TWI*	1B23	--		1A23	BIO00N	TWI
1C24	BIO09N	TWI	1B24	--		1A24	BIO01N	TWI
1C25	BIO10N	TWI	1B25	CUA1		1A25	BIO02N	TWI
1C26	BIO11N	TWI	1B26	OV		1A26	BIO03N	TWI
1C27	BIO12N	TWI	1B27	CUA2		1A27	BIO04N	TWI
1C28	BIO13N	TWI	1B28	CUA3		1A28	BIO05N	TWI
1C29	BIO14N	TWI	1B29	CUA4		1A29	BIO06N	TWI
1C30	BIO15N	TWI	1B30	--		1A30	BIO07N	TWI
1C31			1B31	+5VL		1A31		
1C32	+ 5VL		1B32	+5VL		1A32	+ 5VL	

WDE: UPL-BUS-2 CONNECTOR PIN ASSIGNMENT

* TWI = Two Way Interface
N.C. = Not connected
IP = Input
OP = Output

1.4.2 HARD DISK CONTROL INTERFACE

1.4.2.1 SIGNAL DESCRIPTION

SIGNAL NAME	DESCRIPTION
DIRI	DIRECTION 1N
DS1...3	DRIVE SELECT
STEP	STEP PULSE to move the head 1 track
READY	DISK DRIVE READY FOR USE
INDEX	INDEX, pulse on each revolution, sector 0
HS0...3	HEAD SELECT, to select head 0 ... 15
WRTF	WRITE FAULT
TR0	TRACK 00, heads are on track 00
SEEKC	SEEK COMPLETE, Seek finished after step pulse(s).
WRG	WRITE GATE, Write enable

1.4.2.2 HARD DISK CONTROL CONNECTOR

Connector 3, HDC Interface

	A	B
17	DIR1	L
16		L
15	DS3	L
14	DS2	L
13	DS1	L
12	STEP	L
11	READY	L
10	INDEX	L
9	HS1	L
8		L
7	HS0	L
6	WRTF	L
5	TR0	L
4	SEEKL	L
3	WRG	L
2	HS2	L
1	HS3	DUMMY

1.4.3 HARD DISK DATA INTERFACE

1.4.3.1 SIGNAL DESCRIPTION

SIGNAL NAME	DESCRIPTION	
MRDO... 2	- MFM READ DATA	Drive 0,1 or 2
PRDO... 2	+ MFM READ DATA	Drive 0,1 or 2
MWRDO...2	- MFM WRITE DATA	Drive 0,1 or 2
PWRDO...2	+ MFM WRITE DATA	Drive 0,1 or 2
DRSO ...2	DRIVE SELECTED	Drive 0,1 or 2

1.4.3.2 HARD DISK DATA CONNECTOR

Connector 4, HDO Interface

	A	B
10	DUMMY	L
9	MRDO	PRDO
8	L	L
7	MWRDO	PWRDO
6	L	L
5	L	
4	L	
3	L	
2	L	
1	L	DRSO

Connector 5, HD1 Interface

	A	B
10	DUMMY	L
9	MRD1	PRD1
8	L	L
7	MWRD1	PWRD1
6	L	L
5	L	
4	L	
3	L	
2	L	
1	L	DRS1

Connector 6, HD2 Inteface

	A	B
10	DUMMY	L
9	MRD2	PRD2
8	L	L
7	MWRD2	PWRD2
6	L	L
5	L	
4	L	
3	L	
2	L	
1	L	DRS2

1.4.4 FLOPPY DISK CONTROL INTERFACE 5.25 INCH

1.4.4.1 SIGNAL DESCRIPTION

SIGNAL	DESCRIPTION
IUDCH	IN USE/DISK CHANGE
HSEL	HEAD SELECT
RD	READ DATA
WRPROT	WRITE PROTECT
TRK0	TRACK 00, Heads are on track 00
WRGF	WRITE GATE, Write enable
WRD	WRITE DATA
STP	STEP, steppulse to move heads 1 track
DIRS	DIRECTION
MOTON	MOTOR ON, spindle motor
SEL2	SELECT unit 1
SEL1	SELECT unit 0
INDX	INDEX, pulse on each revolution, sector 0
SEL4R	UNIT READY

1.4.4.2 FLOPPY DISK CONNECTOR 5.25 INCH

Connector 7, FDC Interface

	A	B
17	IUDCH	L
16	HSEL	L
15	RD	L
14	WRPROT	L
13	TRK0	L
12	WRGF	L
11	WRD	L
10	STP	L
9	DIRS	L
8	MOTON	L
7		L
6	SEL2	L
5	SEL1	L
4	INDX	L
3	SEL4R	L
2		L
1		DUMMY

1.4.5 FLOPPY DISK CONTROL INTERFACE 8 INCH

1.4.5.1 SIGNAL DESCRIPTION

SIGNAL	DESCRIPTION
FA8N	FAULT, fault for 8 INCH
RDY8N	READY, ready for 8 INCH
FARE8N	FAULT RESET, fault reset for 8 INCH
LOC8N	LOW CURRENT, low current for 8 INCH

1.4.5.2 FLOPPY DISK INTERFACE 8 INCH CONNECTOR

Connector 8, FDC8 Interface

	A	B
4	DUMMY	FA8N
3	L	RDY8N
2	L	FARE8N
1	L	LOC8N

1.4.5.3 CONNECTION OF 5.25 INCH AND 8 INCH FLOPPY

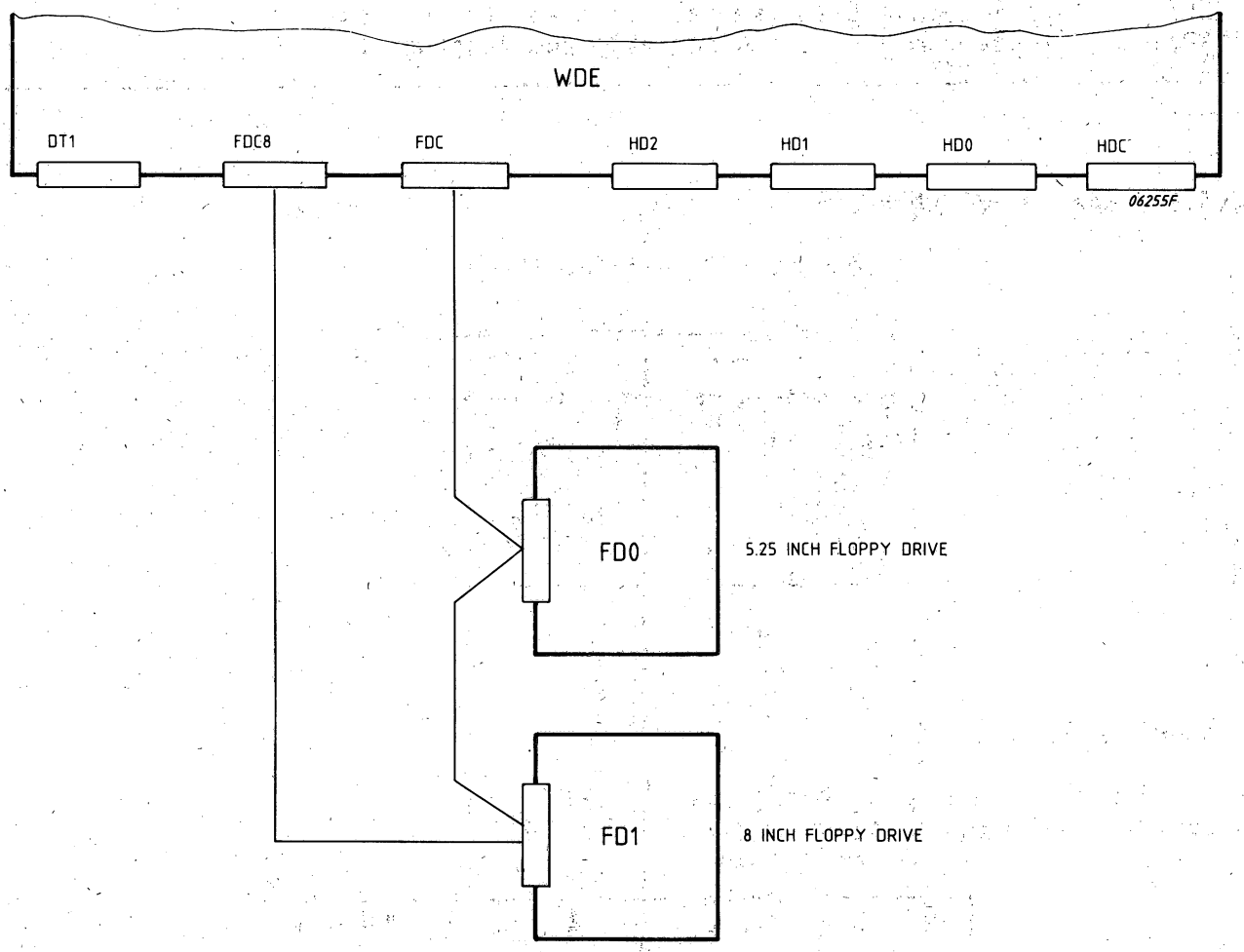

Figure 1.10 CONNECTION OF 5.25 AND 8 INCH FLOPPY

Note: FD0 must be a 500kbit/sec type, than both drives have the same accessparameters.

The 5.25 INCH Floppy Drive must be drive 0, and the 8 INCH Floppy Drive must be drive 1. This for READY detection of the 8 INCH drive, it works only for drive 1. IPL is not possible from the 8 INCH drive, only from FD0.

1.4.6 DTI INTERFACE

DTI is Diagnostic Test Interface

1.4.6.1 SIGNAL DESCRIPTION

SIGNAL	DESCRIPTION
CONNECTN	Diagnostic Tool Connected. Signal from Testtool to WDE.
EMADAN	This signal is used to trigger a DMA cycle. Signal from WDE to Testtool
RESETN	Reset WDE Signal from Testtool to WDE
SDTUN	Received Data (serial) from WDE to Testtool
SDUTN	Transmitter Data (serial) from Testtool to WDE

1.4.6.2 DTI CONNECTOR

Connector 9, DTI Interface

	A	B
5	DUMMY	L
4	L	EMADAN
3	L	RESETN
2	L	SDTUN
1	CONNECTN	SDUTN

1.5 APPLICATION NOTES

The DFP can be used in systems with a UPL-BUS.
A typical application of the DFP is in the P4200.

Rel. Dev. No.	DISK TYPE	1st C.U 11H	2nd C.U 12H
00	FD0	DK3	DK13
01	HD0	DK5	DK15
02	FD1	DK7	DK17
03	HD1	DK9	DK19
04	HD2	DK11	DK21

IPL Controller: only from 1st C.U

FD0 DK3
HD0 DK5

1.6 INSTALLATION

1.6.1 STRAPSETTINGS WDE

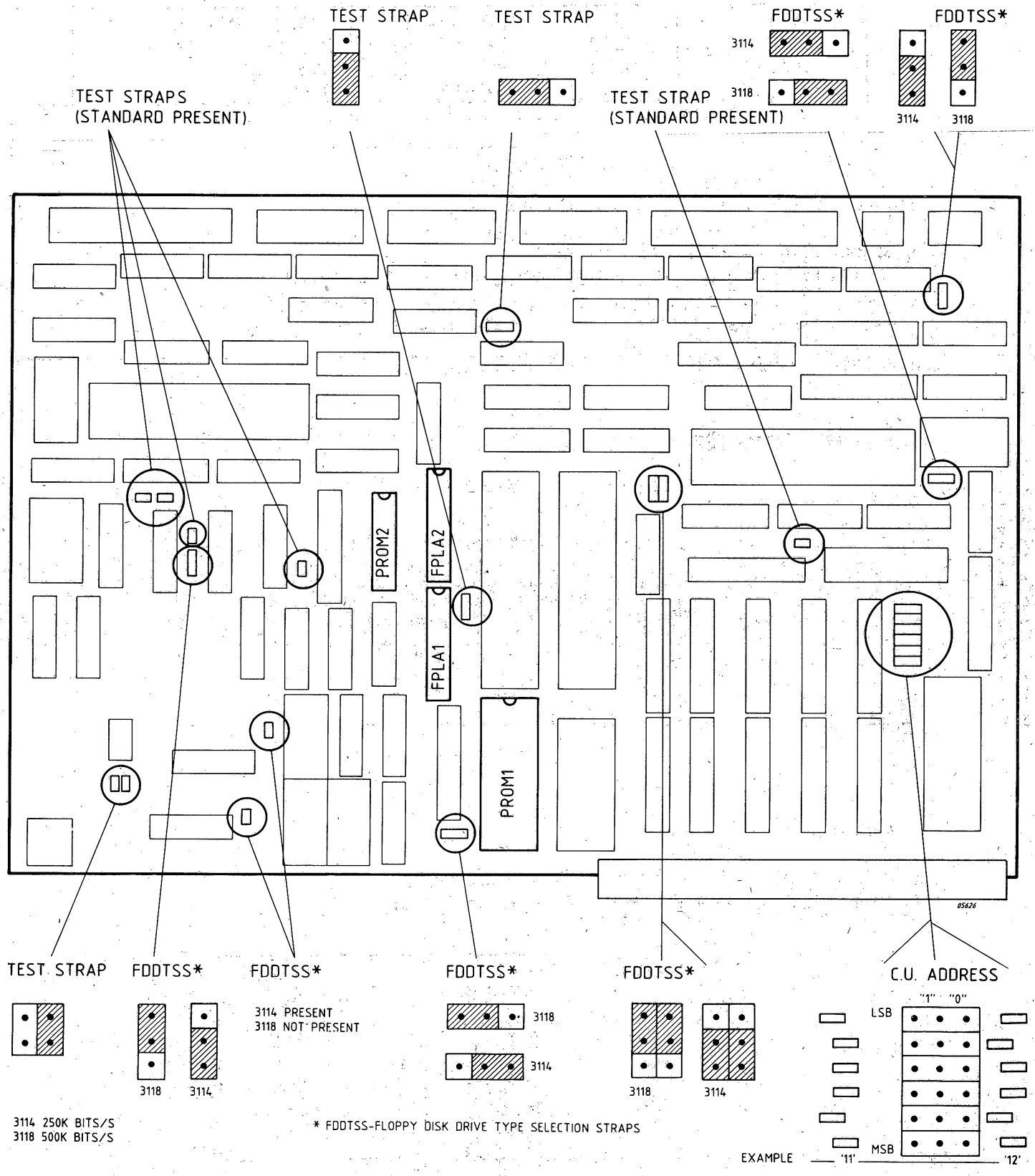

Figure 1.11 STRAPSETTING WDE

1.6.2 PROM TABLE WDE

	LOCATION	IDENTIFICATION	12NC	DESCRIPTION
PROM 1	E3A4	2764-3-012	39472	MPR 5 1/4 DCU
PROM 2	D3C8	82S185-138	39501	PLL PROM
FPLA 1	D8B8	82S153-029	39511	
FPLA 2	D8C9	82S153-030	39521	

1.6.3 MOUNTING

See concerning Field Service Manual
The position in the logic rack is dependant of the machine type.

1.6.4 INTERCONNECTIONS (SEE 1.4 INTERFACES)

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Functional Outline

The DFP is a microprogram controlled direct memory access control unit, whose hardware is controlled by a microprogram resident in a control store.

It is the intention of this functional outline to describe the following topics:

a. The HSI for the DFP
   This topic will contain a description of all the commands executed by the DFP.

b. The Hardware of the DFP at block diagram level
   This topic will contain descriptions of each hardware part with special emphasis on the execution of each part function. Data flow between each individual hardware part will also be discussed.

c. The Microprogram of the DFP at block diagram level

2.1 THE HSI, DMA CONTROL UNITS

2.1.1 GENERAL

Since DMA CONTROL UNITS can read and write in Main Memory, at the Hardware-Software Interface use is made of areas in Main Memory for communication between the software and Control Units.

Only a small amount of direct communication between CPU and DMA Control Units is needed, that is:

1. A CIO START instruction issued by the software to indicate that the Control Unit has to perform some operation.

2. An Interrupt from the Control Unit to the CPU indicating that the Control Unit has to report an event.

3. An SST instruction, issued by software, indicating that the interrupt generated by the Control Unit, has been handled and that the interrupt must be cleared.

Three types of interface areas are defined as follows:

1. I/O DESCRIPTOR (IOD)

   For an I/O operation the software requires to be performed by a Control Unit, an "I/O Descriptor" ("IOD") must be prepared. In the IOD, the software must specify the I/O command to be executed and for which device this has to be done.
   The Control Unit will report any return information generated as a result the execution of an I/O operation in the IOD.

   Note that, in principle, a number of I/O operations may be pending for a particular device; the maximum number will be specified in subsequent sections for each device type.

2. CONTROL UNIT INTERFACE DESCRIPTOR (CID)

   For each Control Unit connected, an interface area must be present; This area is called the "CONTROL UNIT INTERFACE DESCRIPTOR" ("CID").
   The CID must be used during the Initiation of an I/O operation by means of a CIO START instruction, to specify the address of the IOD that describes the I/O operation to be performed.

   In addition, the CID is used by the control unit when an interrupt is given to specify the type of interrupt and, in some cases, to identify the device or I/O operation (IOD) to which it relates.

3. CONTROL UNIT START DESCRIPTOR (CSD)

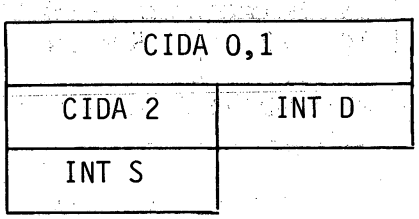
   This area, whose address is identical for all Control Units, is used to specify the real address of the CID. In addition, CSD specifies the interrupt level and destination to be used by the Control Unit if a coded interrupt system is employed.

   Finally, each DMA Control Unit will have a unique address, which is fixed at system installation time. This address must be used as parameter of the CIO START and SST instructions to address the proper Control Unit.

2.1.2 INTERFACE DESCRIPTORS

All three Interface Descriptors are aligned to word boundaries.

2.1.2.1 CSD-LAYOUT



All fields of CSD must be filled by software before the execution of the first CIO START instruction to a Control Unit that has been put into the reset state.

1. CIDA - CID Address (24 bits)

   This field must contain the real word address of the CID to be used by the Control Unit.

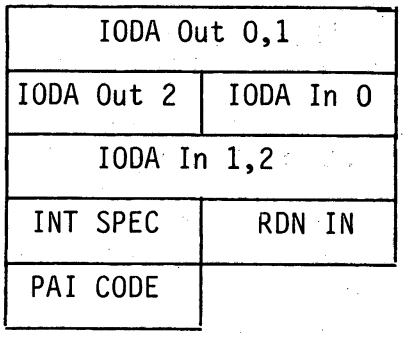
2. INT D - INTerrupt Destination (8 bits)

   This field, also used with a coded interrupt system, identifies the unit to which the Control Unit should direct any interrupts generated. That unit will acknowledge and respond to these interrupts.
   Clearly, this field has a meaning only in a multiple processor configuration, since processors are the only system units issuing CIO START and responding to interrupts.

3. INT S - INTerrupt source (8 bits)

   This field is used when a coded interrupt system is employed to designate the interrupt level to be used by the Control Unit (See 2.1.4 for more details).

2.1.2.2 CID- LAYOUT



1. IODA Out - IOD Address Out (24 bits)

   This field must be filled by software before the execution of a CIO START instruction. It must contain the real word address of the IOD specifying the the I/O operation to be started.

2. IODA In - IOD Address In (24 bits)

   This field is filled by the Control Unit before an I/O Completion Interrupt is given to the CPU. It contains the real word address of the IOD corresponding with the I/O operation that was completed.

3. INT SPEC - INterruption SPECification (8 bits)

   This field is filled by the Control Unit before and interrupt is given to the CPU (See also 2.1.4).
   The meanings of the used codes are:

INT SPEC	TYPE
'80' X	PAI
'40' X	REL
'20' X	IOC

   (1) PAI - Peripheral Attention

   This code is set by the Control Unit before a Peripheral Attention Interrupt is given.

   (2) REL - Release CID

   This code is set by the Control Unit before a Release Interrupt is given.

   (3) IOC - I/O Completion

   This code is set by the Control Unit before an I/O Completion interrupt is given.

4. RDN In - Relative Device Number (8 bits)

   This field is filled by the Control Unit before a Peripheral Attention Interrupt is given to the CPU; it designates the device (by means of Relative Device Number within the Control Unit) from which an attention signal was received.

5. PAI Code - Peripheral Attention Interrupt Code (8 bits)

   This field is filled by the Control Unit before a Peripheral Attention Interrupt is given to the CPU; it contains information on how software should react to the PAI Interrupt.

2.1.2.3 IOD - LAYOUT GENERAL

FIXED PART (6 octads long)	See 2.1.2.4
DEVICE DEPENDENT PART (length depends on device)	See 2.1.2.5
DATA DESCRIPTION/ DATA CHAINING	See 2.1.2.6
DEVICE DEPENDENT PART 2	(magnetic disk only)
COMMAND CHAINING (may be empty)	

Each of these parts contains an even amount of octads.

1. THE FIXED PART

   The fixed part is detailed in 2.1.2.4. It has the same layout for all types of device and for all commands.

2. THE DEVICE DEPENDENT PART

   The device dependent part contains any additional information. Its length is dependent on the type of device: Its layout may even depend on the particular command. In the case magnetic disk, the device dependent part has an extension located behind the data description.
   For details on the device dependent parts see 2.1.2.5 (briefly) and the appropriate sections on the various devices.

3. THE DATA DESCRIPTION

The data description is detailed in 2.1.2.6

(1) NO DATA CHAINING:
In this case the data description area in the IOD may either directly contain the data concerned or a reference (Address) to the data.

(2) DATA CHAINING
The command specified in the IOD involves data transfers to/from a sequence of I/O areas. In such cases, the data description part of the IOD is repeated an appropriate number of times.
Every occurrence of such a description of part of the total amount of data related to the command is called a Data Descriptor.
A "CONTR1" field within this Data Descriptor controls Data Chaining.
Some special cases allow for e.g. the mutual synchronisation of simultaneous I/O processes.
Note that a chain of Data Descriptors may extend outside the IOD.

4. Device Dependent Part 2
This item is present only in case magnetic disk. Its length is fixed: its precise meaning depends on the particular command. See the appropriate sections of this chapter.

5. Command Chaining
The I/O operation consists of the execution of a sequence of commands, specified in a chain of IOD's.
Within each such IOD, Data Chaining as above may be used.

2.1.2.4 IOD LAYOUT, FIXED PART

LAYOUT:

RDN Out	COM
CONTRO	LOGSTAT
PHYSTAT	

Meaning of the various fields:

1. RDN Out - Relative Device number (8 bits)
This field must be filled by software before a CIO START instruction is executed: it designates the device (relative within the Control Unit) for which an I/O operation must be performed.

2. COM - Command Code (8 bits)
This field must be filled by software before a CIO START instruction is executed; it specifies the command to be executed.

3. CONTRO - Control Information (8 bits)
This field must be filled by software before a CIO start instruction is executed; it gives the following information about the command to be executed:

BIT 0 = 0 No command chaining
= 1 Command Chaining

BIT 1 : 7 Reserved for standard control information

4. LOGSTAT - Logical Status (8 bits)
This field will be filled by the Control Unit before an I/O completion interrupt is given.
The Logical Status octad will contain that kind of status information that relates to conditions other than hardware malfunctions.
On HSI level the Logical Status octad has only significance in the following cases:

(1) For peripherals with error recovery in hardware.
(2) For peripheral without hardware error recovery, in case the Physical Status field has a zeroes pattern.

In all other cases the Logical Status octad can have a not significant bit pattern.
If significant, the following values of the Logical Status have a standard meaning for all device types:

(1) Value 0 - NORMALLY ENDED
This bit pattern occurs if there is no bit set in the physical status and if no logical condition should be mentioned.

(2) Value 3 - IRRECOVERABLE ERROR
This bit pattern is only significant if error recovery is performed by hardware. It indicates that the peripheral malfunction could not be recovered with the hardware error recovery procedures.

(3) Value 6 - DEVICE BUSY
This bit pattern occurs if the maximum number of I/O operations that may be outstanding for a device is exceeded.

(4) Value 7 - RDN NOT PRESENT
This bit pattern occurs if a CIO START instruction was performed with a non existing Relative Device Number in the IOD.

(5) Value 8 - CU ERROR
This bit pattern indicates that there is a malfunction with the Control Unit or in a peripheral device whose number cannot be determined.

(6) Value 32 - COMMAND REJECTED

This bit pattern indicates that the specified Command Code does not exist for the peripheral designated in the RDN Out field in the IOD, or is not allowed at this moment.

5. PHYSTAT - PHYSICAL STATUS (16 BITS)

This field will be filled by the Control Unit before an I/O completion interrupt is given.

The physical status octads will contain that kind of status information relating to malfunctions of the peripheral and/or the controlling hardware.

For peripherals that have their error recovery actions completely programmed in software, a malfunction will directly lead to bit settings in the physical status octads and termination of the I/O operation by means of an I/O completion interrupt.

For peripherals that have their error recovery actions (maybe partly) performed in hardware, a malfunction causes a number of retry actions to be performed in hardware and the I/O operation is only terminated after the retry action is successfully completed or the number of (unsuccessful) retries has reached a predefined maximum value.
If the retry was unsuccessful the value of the Logical Status octad is set to 'irrecoverable error', if successful this condition will not be set.

In both cases (successful or not successful), the number of Retries will be mentioned in a field called "Number Of Retries" ("NOR") in the device dependent part of the IOD. In general, the retries field indicates the sum of all the retry actions for one I/O operation.

The physical status octads will indicate all error conditions that have occurred during the execution of the I/O operation, including the hardware retry actions.

In the Physical Status, the following bits have a standard meaning for all peripherals:

(1) Bit 1 of octad 0 - PARITY ON PERIPHERAL INTERFACE
This bit is set if a parity error on the interface lines at the peripheral side had been defected.

(2) Bit 6 of octad 0 - PERIPHERAL NOT OPERABLE
This bit indicates that the peripheral is present, but cannot be used because, e.g.: no power, no paper, cover not closed. It is possible that other bits of the status octads specify the situation in more detail in a peripheral dependent way.

(3) Bit 0 of octad 1 - SYSTEM PARITY ERROR
This bit is set if a parity error is detected at the system side of the interface that connects the peripheral with the system.

(4) Bit 1 of octad 1 - SYSTEM TIME OUT
This bit is set if the system can no longer communicate with the peripheral because of time out conditions.

2.1.2.5 IOD LAYOUT, THE DEVICE DEPENDENT PART

This part has neither a fixed length nor a fixed layout. Reference should be made to the appropriate test per device. However, two fields within the device dependent part are of such a general nature that they had better be mentioned here. They are:

1. IOAL - I/O Area Length (16 or 32 bits)
   This field must be filled by software before a CIO START instruction is executed and has the following meaning:

   (1) In case no data chaining is used it designates the length of the I/O area minus one.
   (2) In case data chaining is used it designates the total length minus one of the data to be transferred with this command.

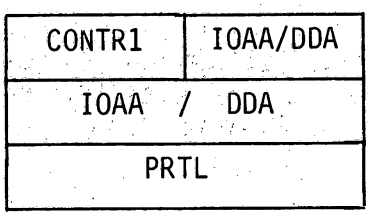
2. REML - REMaining Length (16 or 32 bits)
   This field will be filled by the Control Unit before and I/O completion interrupt is given; its value is the initial value of the IOAL field minus the actual number of data octads transferred during the execution of the I/O command. Note that a value 'FFFF'X or 'FFFFFFFF'X in this field designates a remaining length of zero octads.

Note: Usually these two items overlap (are located in the same field).

2.1.2.6 IOD LAYOUT, DATA DESCRIPTION

In case "NO DATA CHAINING", this part of the IOD contains only one "DATA DESCRIPTOR"; in case "DATA CHAINING" there is a series of such descriptors. That series may even from some point be continued elsewhere in the memory.

LAYOUT OF A DATA DESCRIPTOR



Control octad;
IO Area Address or
Data Descriptor Address

Partial Length
(Not present if only one element)

2.1.2.7 LOCATION OF THE CSD

The Control Unit Start Description (CSD) must be located by software at a word address below 64K octads. This address is identical for all Control Units.

The CSD contents must be prepared by software and will subsequently be fetched and remembered by the Control Units.

The transfer procedure is as follows:

1. If a Control Unit is in the RESET STATE (see 2.2.1), the real address of its CID as well as interrupt level and destination must be put in CSD and the real address of CSD must be specified at a fixed location in Main Memory (octad addresses '80' X and '81' X) when the first CIO START for it is issued.
   First the Control Unit will fetch the CSD address from locations '80' X and '81' X. Then it will fetch the contents of CSD and retain them for use with subsequent I/O operations.

2. The CSD contents, as kept within the Control Unit, are no longer valid after a hardware reset or after the execution of a 'TERMINATE' command. These two events force the Control Unit in the 'RESET' state.
   More details on the 'TERMINATE' command can be found in 2.2.1.

2.1.3 USAGE OF I/O INSTRUCTIONS

2.1.3.1 CIO - START

The CIO-START instruction is used by software to indicate that the addressed Control Unit has to perform an operation.

Before the CIO START instruction is executed (with the proper Control Unit address as parameter), the CID must be filled with the address of an IOD describing the operation to be performed.

In some cases also the CSD must be set up as described in 2.1.2.1 and the CSD address must be loaded in locations '80' X and '81' X before executing a CIO START (see 2.1.2.7 and 2.2.1)

2.1.3.2 SST

Following an interrupt from a Control Unit software must, after having extracted the proper information from the CID, execute an SST instruction, with the Control Unit number as parameter. This indicates to the Control Unit that the interrupt has been received, the Control Unit can clear its interrupt and the CID is available again for the generation of another interrupt.

2.1.3.3 TST

The TST instruction is not available for use with DMA Control Units: If a TST instruction is executed, it will have the same effect as an SST instruction.

2.1.4 INTERRUPTIONS

2.1.4.1 TYPES OF INTERRUPTS

A DMA Control Unit may generate three types of interrupts as follows:

1. RELEASE INTERRUPT

   This type of Interrupt is a reaction to a CIO START instruction. It indicates that the CIO START parameter (IOD address) has been retained by the Control Unit; i.e. the CID can be released (and can be used to initiate another I/O operation for this Control Unit).

2. PERIPHERAL ATTENTION INTERRUPT

   This type of interrupt occurs it one of the devices, connected to a Control Unit changes state (e.g. from inoperable to operable or vice versa). The Relative Device Number of this device is specifed in the CID.

3. I/O COMPLETION INTERRUPT

   When an I/O operation has been completed, the related status information is placed in the proper IOD and the Control Unit sends an I/O completion interrupt to the CPU, with the IOD address placed in the 'IODA IN' field of its CID.

These three possibilities are coded in the field 'INT SPEC' of the CID (see 2.1.2) by the Control Unit before it generates an interrupt.

2.1.4.2 INTERRUPT LEVELS

Depending on the hardware interrupt system used, there are two ways in which the interrupt level for the above mentioned interrupts can be determined:

1. WIRED INTERRUPT SYSTEM

   In this case each Control Unit has one unique interrupt level which it uses for all its interrupts. This interrupt level is fixed by wiring at system installation time.

2. CODED INTERRUPT SYSTEM

   In this case interrupt levels are not fixed by wiring and must be specified by software in the field 'INT S' of CSD once with the initial 'TEST CU' Command (See 2.2.1).

2.1.4.3 INTERRUPT DESTINATION

This applies to coded interrupt system only and it is an extension of the mechanism to allow the introduction to the system of more processors that can participate in the interrupt scheme.

The identification of the processor that will respond to interrupts generated by a Control Unit must be specified by software in the field 'INT D' of CSD once with the initial CIO 'TEST CU' command issued to that Control Unit.

2.2 THE HSI, I/O COMMANDS FOR DMA CONTROL UNITS

2.2.1 STANDARD I/O COMMANDS

The command code in the IOD specifies which operation must be performed by the Control Unit.
Most of these commands are device dependent; some of these commands however have a more general meaning. These commands are 'IPL', 'TEST CU' and 'TERMINATE'.
The 'IPL' command is only known by Control Units, which have the possibility to operate as IPL Control Unit.

The effect of these commands can be seen, if we look at the State Diagram of a Control Unit (see figure below).

Each Control Unit knows two states: the 'RESET' STATE and the 'NORMAL OPERATION' STATE; an IPL-Control Unit knows still one state more: the 'IPL' STATE.

1. 'RESET' STATE

   Following a hardware reset or the execution of a 'TERMINATE' command, the Control Unit enters the 'RESET' STATE and stays there until it receives a CIO START. This first CIO START implies that the CSD address can be fetched from locations '80'X and '81'X in Main Memory (See 2.1.2.7), followed by the fetching of the contents of CSD.
   The command code in the IOD related to this CIO START, must be 'IPL' or 'TEST CU.
   If an other command is specified, the Control Unit generates an IOC interrupt with 'COMMAND REJECTED' in the Logical Status field of the IOD and remains in the 'RESET' STATE.

   In the 'RESET' STATE the Control Unit will be passive, i.e. it will not generate any interrupts or access Main Store.

2. 'IPL' STATE

   After detection of the 'IPL' command, the IPL Control Unit enters the 'IPL' STATE and performs the proper IPL actions. If new CIO START instructions are executed while the Control Unit is in the 'IPL STATE, these will be neglected.
   After completion of the 'IPL' command the Control Unit enters the 'RESET' STATE.

3. 'NORMAL OPERATION' STATE

   After execution of the initial 'TEST CU' command, and if the test for the functioning of the Control Unit is successful (no errors are detected), a Control Unit enters the 'NORMAL OPERATION' STATE.

   The handling of the other CIO START instructions will normally be done in this state.

EVENT	C. U. STATES		
	'RESET'	'IPL'	'NORM. OPER'
HARDWARE RESET	-	S:= 'RESET'	S:= 'RESET'
CIO 'IPL' for IPL - CU	S:= 'IPL'	Ignored	COMMAND rejected
CIO 'IPL' for others	Command rejected	not appl.	Command rejected
Completion of IPL	not appl.	S:= 'RESET'	not appl.
CIO 'TEST CU'	If test is successful then: S:= 'NORM. OPER.' Else: -	Ignored	Test C. U. Functioning
CIO 'TERMINATE'	Command rejected	Ignored	S:= 'Reset'
Other CIO's	Command rejected	Ignored	-

STATE CHANGES of DMA Control Units

DESCRIPTION OF THE STANDARD COMMANDS:

The codes '80' X thru '87'X are reserved for standard commands.

2.2.1.1 TEST CU - '80' X -

This command may be given to a Control Unit while it is in the 'RESET' or 'NORMAL OPERATION' state.
It will cause the Control Unit to perform the following actions:

(1) In 'RESET' and 'NORMAL OPERATION' state
The Control Unit will execute an internal test sequence to check its correct functioning. The result of this test is reported in the status fields of the IOD.

(2) In 'RESET' state only
The Control Unit will fetch the CSD address from locations '80' X and '81' X in memory followed by the fetching of CSD contents, which will be retained for subsequent use.
The 'CIDA' of CSD is used by the Control Unit for accessing its CID.
If the Control Unit uses the coded interrupt system the 'INT S' and 'INT D' fields of CSD are used as interrupt source (level) and destination codes respectively for PAI, REL and IOC interrupts.

After the execution of the 'TEST CU command, and if no functioning error is detected in the test sequence, the Control Unit enters the 'NORMAL OPERATION' state.
No pending peripheral attention interrupts will be issued and pending CIO START instructions will be handled, only if the Control Unit accepts pending CIO's.

2.2.1.2 IPL - '82'X -

This command may be given for an IPL-Control Unit and only if the Control Unit is in the 'RESET' STATE.
The Control Unit enters the 'IPL' state and performs the following actions:

(1) Execute an internal test sequence as for the 'TEST CU' command.
(2) It performs the proper IPL actions.

On completion of the 'IPL' command the Control Unit sets the field 'INT SPEC' in its CID to '20'X (I/O Completion), but does not generate an interrupt. This implies that the field 'INT SPEC' must be cleared before the IPL command is issued and completion must be tested by inspecting the value of this field.
After completion of the IPL command, the Control Unit re-enters the 'RESET' state.

2.2.1.3 TERMINATE - '81'X -

This command may only be given if the Control Unit is in the 'NORMAL OPERATION' state.
After detection of 'Terminate' command, it enters the 'RESET' state.
This implies that I/O operations that are pending at the moment the Terminate command is detected, are not completed.

2.2.1.4 READ IDENTIFICATION - '83'X -

This command may only be issued if the Control Unit is in the 'NORMAL OPERATION' state. The state is not changed. This command fetches a Control Unit dependent identification, to be stored into the I/O area. The command is stopped if the I/O area is completely filled (IOAL) or if no information is present anymore. REML indicates the number of characters not transported.
Layout of the I/O area:

Octad 0-5 : 12NC (12 Hexadecimal digits ('0' - '9'))
Octad 6-end : Control Unit dependent information

2.2.2 NORMAL COMMANDS AND IOD LAY-OUT

NOTES

1. Defective and bad track handling
   If Defective/alternate track handling is supported:
   If a track is defective then alternate is taken but the next track is chosen as if the defective track was not defective.

   If bad track handling is supported:
   If a bad track is detected then from the bad track on the track set with the next higher number is taken.

   In both cases the following is true:
   If this (alternate or next) track is lying outside the cylinder boundaries as specified by the SIO instruction, this will not be considered as a File Protection error.

2. Certain commands may involve more than one sector. However, sectors of different length should not be involved in one command.

2.2.2.1 READ DATA Command Code : '00'X

This command provides for reading of the data field of the sector, that is indicated by the RSN-field in the IOD; reading is continued with the next logical sector(s) until the IO-Area as indicated in the IOD is completely filled. A "Flexible disk unit" will also stop reading when a "deleted data address mark" is encountered (in case of format IBM type 1).

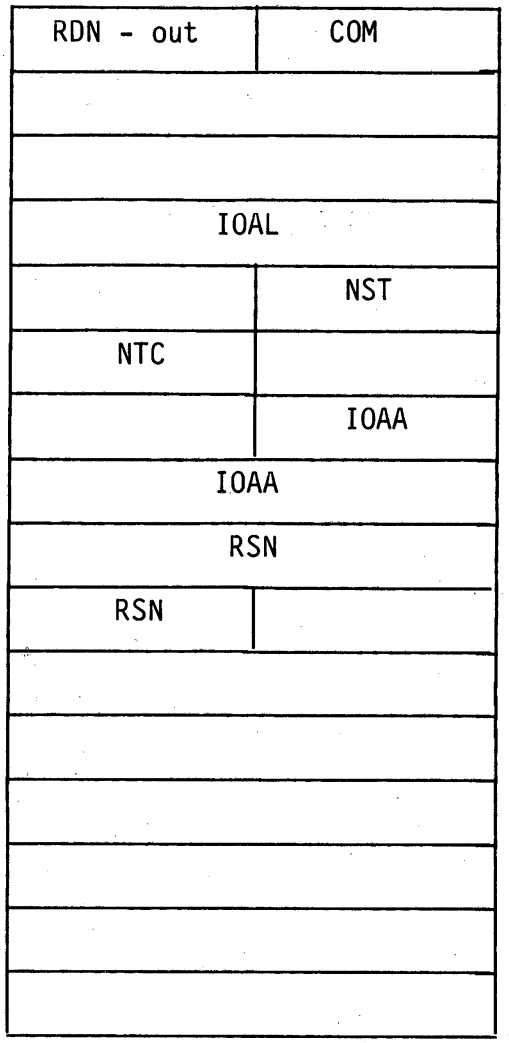
This command can read more than one sector, and per sector, only the data field (128 or 256 octads, depending on the type of disk).

Reading the data field of the first sector starts at the beginning of the data field. It is possible that the data field of the last sector is not completely read, because reading is continued until the IO-Area is completely filled.

In exceptional conditions, the number to be found in the REML-field of the IOD will indicate the part of the IO-Area that is not filled with octads, expressed in octads minus one.

Both the check octads of the sector identifier and the data block of the sectors will be tested.
The unit of information that is transported by this 'READ' command is 8 bits.

IOD Lay-out (shown one word per line), at command:



Relative Device Number, Command

IO Area Length (Octads-1)

Number of sectors per track

Mode; nr of tracks/track set *)

IO Area Address (octad, real)

Real Sector Number

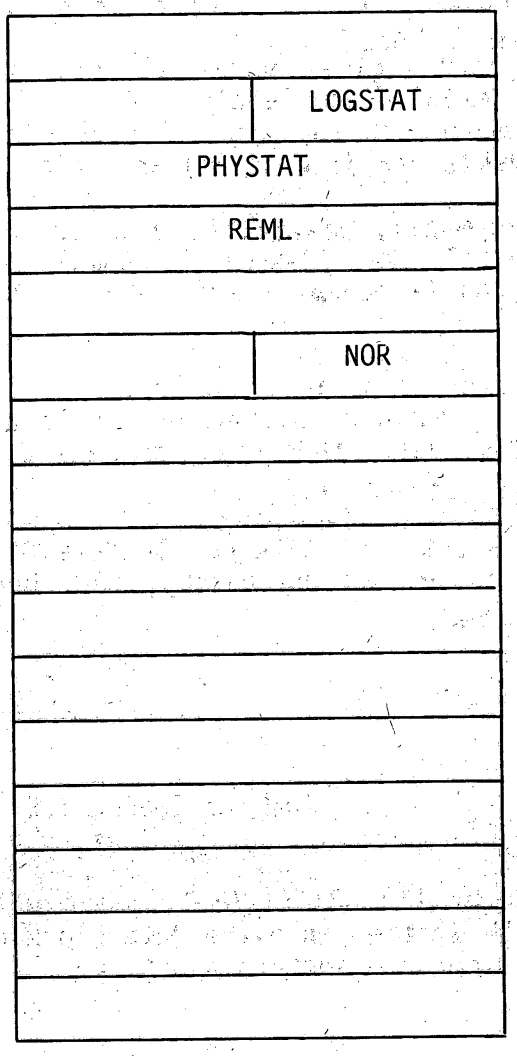
*) FXD/RMD/CMD

Bit	meaning
0	1=Fixed of RMD/CMD 0=Other
1	Reserved for hardware (must be zero)
2:7	NTC

Other disks

Bit	meaning
0	0=Flexible 1=MDD
1	0=Single 1=Double Density
2	0=PHILIPS 1=IBM Format
3	Claimed for extension
4:7	NTC (NR of tracks/set)

At Interrupt:



Logical Status

Physical Status

Remaining Length (octads-1)

Number Of Retries
(not for FXD/RMD)

2.2.2.2 WRITE DATA Command Code : '01' X

The 'WRITE DATA' command provides for writing data into the data field of the sector indicated in the RSN-field in the IOD;
Writing is continued at the data field of the next logical sector(s) until the IO-Area as specified by IOAA and IOAL fields is emptied completely.
The data field contains 128 or 256 octad, depending on the type of disk. Note that, per sector, complete data blocks (see details per disk type) are written.

If the data field of the last sector cannot completely be written with IO-Area information (because writing is continued until the IO-Area is completely emptied), the remaining part of the data field is filled with all zero octads. ('00'X).

The check octads are written by hardware after each data field written.
The number to be found in the REML-field will indicate the number of octads (minus one) not transported from the IO-Area. Obviously, this piece of data will only be meaningful in exceptional cases.

The unit of information that is transported is 8 bits. In case of Flexible Disk or Mini Fixed Disk, a read after write check is done during which a CRC check all sectors written will be performed.

IOD Lay-Out: See 'READ DATA'

2.2.2.3 WRITE DELETED DATA ADDRESS MARK Command Code : 'OE' X
(Flexible Disk, MDD only)

The function of this command is similar to that of the WRITE DATA command with the exception that a "DELETED" indication will be written into the data block of the sector(s) concerned. For details see the appropriate sector layout.

2.2.2.4 SEARCH KEY EQUAL Command Code : '02

This command is defined on a series of (fixed length) "RECORDS". The command is not defined for "sectors" of 128 octads.

The data field of a sector on disk may contain one or more such records. Records are mapped on sectors without any inter record space: the first octad of a record immediately follows the last octad of its predecessor.

If records have a length RL, then "sector length modulo RL" octads at the end of the "sector" are ignored for the purpose of searching.

Searching is carried out on a record-by-record basis, per record proceeding as follows:

. The IO-Area in Main Store, indicated by the IOD, contains a "key-field".

Each record should be considered as containing:

- a key (Length KL+1, as indicated in the IOD).
  The maximum value for KL is 31 (key contains 32 octads).
- 4 extra octads
- data (length DL +1, as indicated in the IOD)
  Thus, the length per record is KL + DL + 6, obviously with a maximum of 256.

Octads numbered KD thru KL from key-field and record are compared.
(KD = "Key Displacement", indicated in the IOD)

Picture of a record:



If the compare on a certain record is not successful, the next record is investigated, either within the same sector or in the next; either within the same track or in the next.
The total number of sectors to be searched is indicated by the NOS-field (Number of Sector) in the IOD. If the search over the mentioned number of sectors is not successful this fact is reflected in the Logical Status.

If the search is successful, this is also reflected in the Logical Status. The identification of the record is transported to the IOD. The identification consists of a Return Real Sector Number (RRSN) and a Sector Displacement (SD) expressed in octads relative to the first octad of the data field.

The ADL-field has no meaning.

IOD Lay-out (shown one word per line), at command:

RDN - out	COM	Relative Device Number, Command
NOS		Number of Sectors-1
	NST	Number of sectors per track
NTC		Mode; nr of tracks/track set *)
	IOAA	
IOAA		IO Area Address (octad, real)
RSN		
RSN	KD	Real Sector Number Key Displacement (octads)
KL	DL	Key Length (ocatds-1) Data Length (octads-1)
ADL		Avail. Data Length (Octads-1)

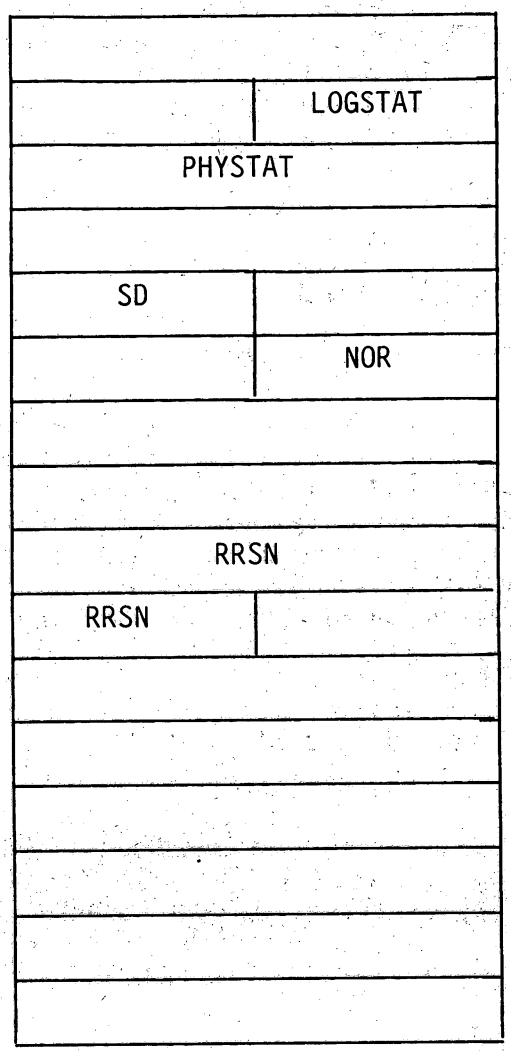
*) FXD/RMD/CMD

Bit	meaning
0	1=Fixed of RMD/CMD 0=Other
1	Reserved for hardware (must be zero)
2:7	NTC

Other disks

Bit	meaning
0	0=Flexible 1=MDD
1	0=Single 1=Double Density
2	0=PHILIPS 1=IBM Format
3	Claimed for extension
4:7	NTC (NR of tracks/set)

At Interrupt:



Logical Status

Physical Status

Sector Displacement (octads)
(if successful)
Number Of Retries
(not for FXD/RMD)

Return Real Sector Number
(if successful)

2.2.2.5 SEARCH KEY EQUAL WITH DATA RETURN Command Code : '03'X

The search operation is performed in the same way as specified for the 'SEARCH KEY EQUAL'. However, if the search is successful, not only the record identification is placed in the IOD, but also the data of the record (for which the search was successful) is placed in the IO-Area, at position IOAA + KL + 5. A data field of ADL+1 octads is returned, even if ADL (available data length as specified in the IOD) is not equal to DL.

IOD layout: see 'SEARCH KEY EQUAL'

2.2.2.6 SEARCH KEY HIGH Command Code : '04'X

The command is the same as the 'SEARCH KEY EQUAL' except for the compare action. If the binary value of the octad as found on the disk has a higher value compared to the corresponding value in the key-field (in the IO-Area) the search is successful; if the binary value of the octad as found on the disk has a lower value the search on this key is unsuccessful; if the binary value of the octad as found on the disk has an equal value the search is undecided and the next octad should be investigated if available; if not the search on this key is unsuccessful. The ADL-field has no meaning.

IOD layout: see 'SEARCH KEY EQUAL'

2.2.2.7 SEARCH KEY HIGH WITH DATA RETURN Command Code : '06'X

The search operation is performed in the same way as specified for 'SEARCH KEY HIGH'.
The return information is of the same category as defined for 'SEARCH KEY EQUAL WITH DATA RETURN'.

IOD layout: see 'SEARCH KEY EQUAL'

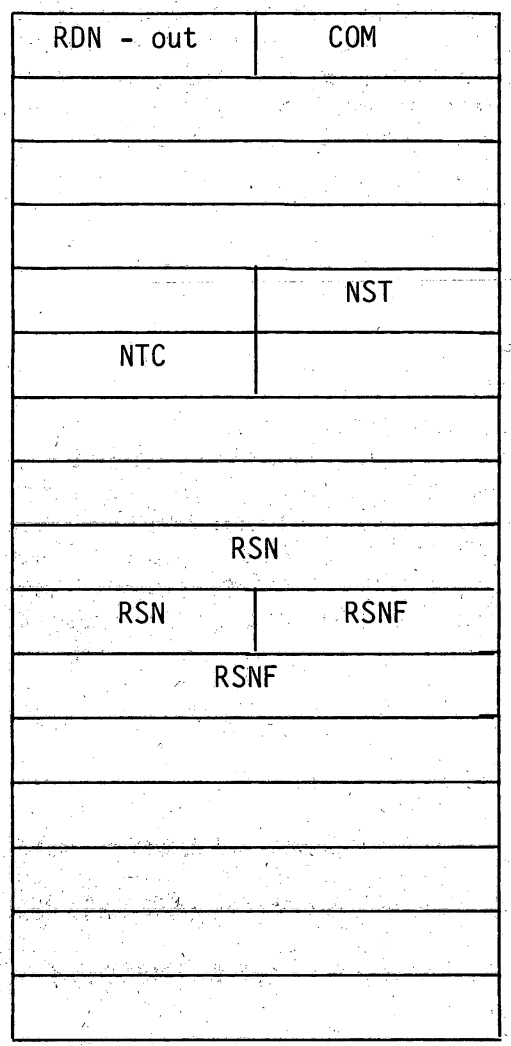
2.2.2.8 FORMAT TRACK Command Code : '05'X
(not for Flexible Disk)

This command will write the gaps, the sector identifiers and data blocks occurring on one track.
The track on which this command should operate is the track denoted by RSN (Real Sector Number) as indicated in the IOD. The identifier is composed by hardware with a flag octad, indicating a non-defective track, the data field is composed by hardware by writing 256 all ones octads.
After the whole track has been written, the sector identifiers and data blocks are checked with the previously written check octads.
The RSNF-field has no meaning

Note for hardware:

Sector number zero can be written on any location of the track. So the following procedure for the localisation of sector number zero is recommended:
If 'FORMAT TRACK' should operate on track number N, first the sector with the highest number should be traced on track number N-1, after which a seek is executed to track number N, where a start can be made with writing of sector number zero. This procedure will guarantee a continuous read, write or search action, going from track N-1 to track N.

IOD Lay-out (shown one word per line), at command:



Relative Device Number, Command

Number of Sectors per track

Mode; nr of tracks/track set *)

Real Sector Number

RSN to Format with

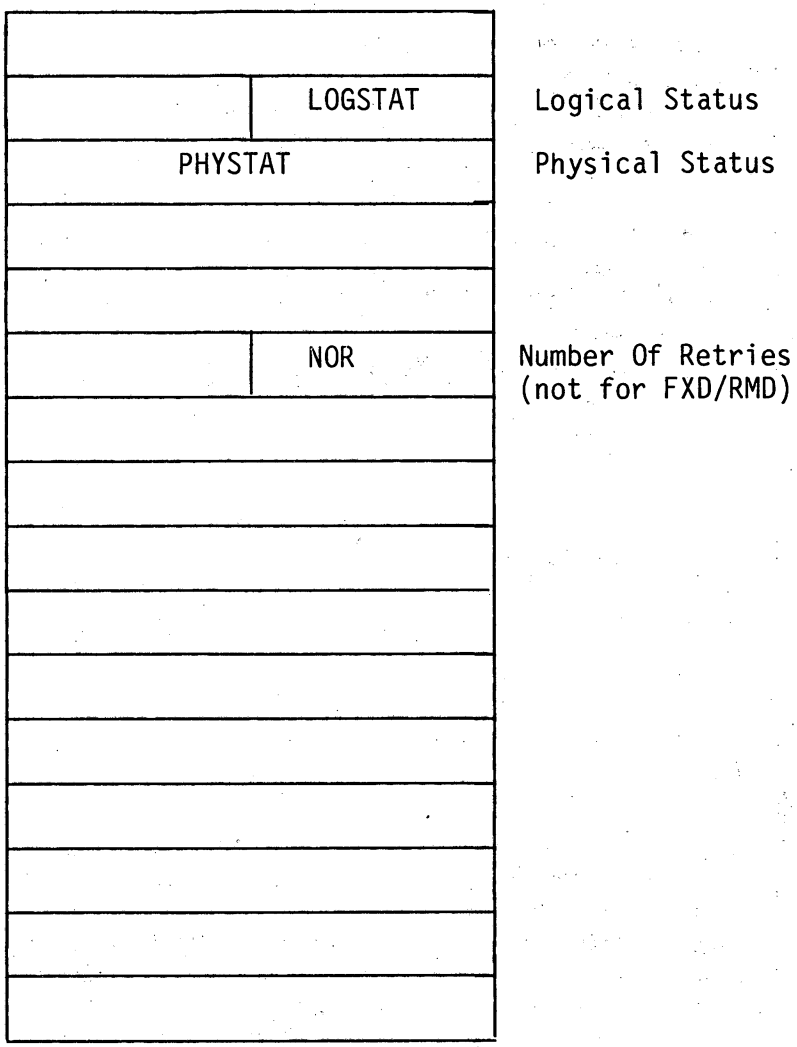
*) FXD/RMD/CMD

Bit	meaning
0	1=Fixed of RMD/CMD 0=Other
1	Reserved for hardware (must be zero)
2:7	NTC

Other disks

Bit	meaning	
0	0=Flexible	1=MDD
1	0=Single	1=Double Density
2	0=PHILIPS	1=IBM Format
3	Claimed for extension	
4:7	NTC (NR of tracks/set)	

At Interrupt:



2.2.2.9 FORMAT DEFECTIVE TRACK (not for Flexible Disk) Command Code : '07'X

This command will write at least one correct identifier with a flag octad denoting that this track is a defective track.
The track on which this command should operate is the track denoted by the Real Sector Number (RSN), as indicating in the IOD. The address of the alternate track as occurring in the identifier is also given as Real Sector Number (RSNF) in the IOD.
With the help of this information the complete identifier is composed by hardware. After the identifiers have been written, they are checked with the previously written data check octads. The command is considered to be executed correctly if at least one identifier is written without errors.
Disk units exist for which defective track and format alternate track cannot be separated. For these disk units the command 'FORMAT DEFECTIVE TRACK' will act as a "NO - OP".

Note for software:
If a track is defective, its alternate track should have the same head number. The head numbers will not be checked by hardware.

IOD layout: SEE 'FORMAT TRACK'

2.2.2.10 FORMAT ALTERNATE TRACK (not for Flexible Disk) Command Code : '08'X

This command will write the gaps, sector identifiers and data blocks occurring on one track. The track on which this command should operate is the track denoted by the Real Sector Number (RSN) in the IOD.
The identifier is composed by hardware with a flag octad indicating an alternate track. The address of the defective primary track, for which this track is a replacement and as occurring in the identifier of this track, is also given as Real Sector Number (RSNF) in the IOD. With the help of this information the complete sector identifier is composed by hardware. The data field is composed by hardware by writing 256 all ones octads.

After the whole track has been written, the sector identifiers and the data blocks are checked with the previously written check octads.
Disk units exist for which format defective track and format alternate track cannot be seperated.
For these disk units the command 'FORMAT ALTERNATE TRACK' will include formatting of the defective track as described below:

This command will also write at least one correct identifier with a flag octad denoting that this is a defective track. The track on which this command should operate is the track denoted by the Real Sector Number (RSNF), as indicated in the IOD. The address of the alternate track as occurring in the identifier is also given as a Real Sector Number (RSN) in the IOD.

With the help of this information the complete identifier is composed by hardware. After the identifiers have been written, they are checked with the previously written check octads. The command is considered to be executed correctly if at least one identifier is written without errors.
Note for software:
If a track is defective, its alternate track should have the same head number. The head numbers will not be checked by hardware.

IOD lay-out: see 'FORMAT TRACK'

2.2.2.11 UNLOCK Command Code : '09'X

This command makes it possible for the operator to change the catridge. After any other IO command requiring a "SEEK" operation, given for the cartridge disk of the related disk drive, the cartridge will be locked and the possibility for the operator to change the cartridge disk will be disabled.

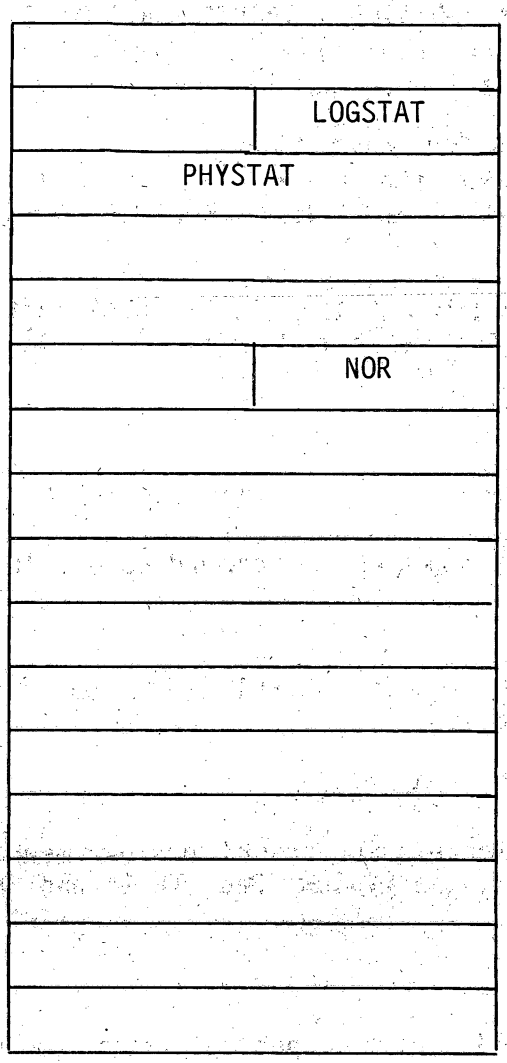
Note: 1. If the command 'UNLOCK' is given for the fixed disk in a fixed disk/removeable disk unit, then the removeable disk will be unlocked just as well.
2. After 'UNLOCK' has been given, the state of the cartridge disk will not be changed by an IO command for the related fixed disk.
3. For disks not having the "LOCK" option, this command will act as a "NO - OP".
4. Logical Status zero will always be reported.

IOD Lay-out (shown one word per line), at command:

RDN - out	COM	Relative Device Number, Command
	NST	Number of Sectors per track
NTC		Mode; nr of tracks/track set *)

*) FXD/RMD/CMD Bit	meaning	Other disks Bit	meaning
0	1=Fixed of RMD/CMD 0=Other	0	0=Flexible 1=MDD
1	Reserved for hardware (must be zero)	1	0=Single 1=Double Density
		2	0=PHILIPS 1=IBM Format
		3	Claimed for extension
2:7	NTC	4:7	NTC (NR of tracks/set)

At Interrupt:



Logical Status

Physical Status

Number Of Retries
(not for FXD/RMD)

2.2.2.12 TEST OPERABLE (TOPER) Command Code : '0A'X

This command causes the transfer to the field "PHYSICAL STATUS" in IOD of the following actual status conditions from disk:
Unsafe 1, Unsafe 2 and Not Operable.

Note: No recovery on these error conditions is done by hardware.
This command does not lock the disk drive.
A possible condition "HAS BEEN NOT READY" will be reset by this command. (CDC drives and MDD only).

Note: For CDC drives, the condition "HAS BEEN NOT READY" will be reset *after* the reporting of the condition at a "TOPER" command. This allows detecting volume changes in combination (FXD/RMD) drives.

IOD lay-out : see 'UNLOCK'

2.2.2.13 INDIACTE ACCESS PARAMETERS Command Code : '0B'X

a) MDD and Flexible disk only)

The function of this command is to transport to the Control Unit, bad track numbers of a disk volume already mounted on a drive.

The bad track numbers are taken from the IOD (P.T.O).

Note: In case of no bad tracks or formats where "bad track" has no meaning (MMD, Flexible Disc with philips format). The fields "Bad TR 1" and "BAD TR 2" have to be filled with 'FF'X.

b) (Certain disk units only see 2.2.8 and 2.2.9)

The function of this command is to transport drive dependant data to the controller.
This command must be given per RDN before commands which handle data other than IPL are given, else the default values will be used.

The parameter are the following:

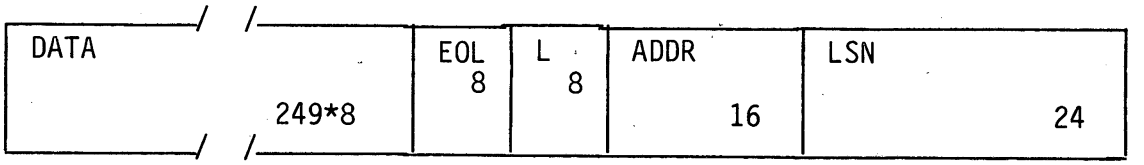
Name	Meaning	Default
NOC	Number of Cylinders	192
NOH	Number of Heads	8
SRWCC	Start Reduced Write Current Cylinder number	96
SWPCC	Start Write Pre-Compensation Cylinder number	0
ECCM	Max ECC-length	11
INTERL	Interleave factor	4
STEP	STEP rate code	0

IOD Lay-out (shown one word per line), at command:

RDN - out	COM	Relative Device Number, Command
	BAD TR 1	Number of BAD Track 1
BAD TR 2		Number of BAD Track 2
NOC		Number of Cylinders
NOH	SRWCC	Number of Heads, Start Red. Write Current
SRWCC	SWPCC	
SWPCC	ECCM	Start Write Pre Comp., ECC Length
INTERL	STEP	INTERLeave factor, STEP rate code

At Interrupt: as with "TOPER".

This command provides for the transport of the contents of a certain number of data fields to certain locations in main store.
The first data to be transported lies in the second indicated sector. The first indicated sector is found with help of the Real Sector Number (RSN), given in the IOD.
If a track is defective the alternate track is chosen, but the next track is chosen as if the defective track was not defective.
The layout of the data fields on the disk used for "Program Load" is fixed and will have the following Layout:



DATA - This field or part of this field should be transported to an IO-Area *).

EOL - End Of Load
If bit 7 of this octad is one, the data as found in the same data field as EOL *) is the last piece of data to be transported.
If bit six of this octad is one, it indicates that the next to be loaded sector has as address the current Logic Sector Number increased with 2.

Note: If bit 6 is one, then the Logical Sector Number as found in the same data field as this bit should contain the current Logic Sector Number + 2.

L - Length
L + 1 is the number of octads to be taken from the data of the next sector.

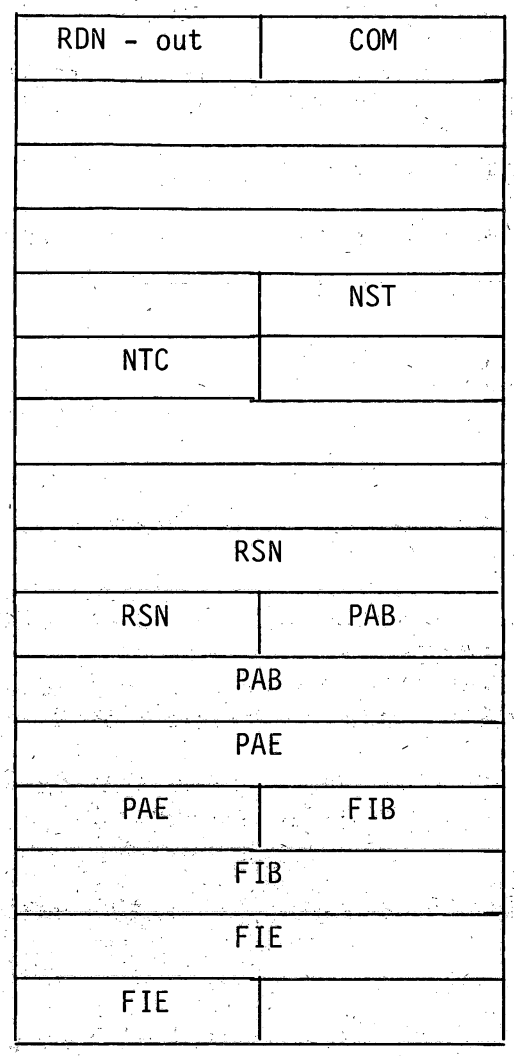
ADDR - Next ADDRess
This field contains a logical address, which will be made real with help of the address parameters 'PAB' and 'PAE' in the IOD.
PAB is the real address of the first octad of the store area for which the load command is executed.
PAE is the real address of the octad of that area.

The real next address found by adding PAB and addr denotes the begin address of the area in main store where the data field of the next sector is transported to.
Still all these areas in Main Store should lie within the area indicated by PAB and PAE, otherwise the load will be stopped or not be executed and memory protection will be set in the Logical Status.
Memory protection appears when PAB+ADDR+L greater than PAE.

LSN - Logic Sector Number
This field denotes the Logic Sector Number of the next sector where the data is to be found for the load operation. LSN gives a displacement of sectors; the base is 'FIB' so the Real Sector Number can be calculated by adding FIB and LSN.
Because the new sector number should lie within the file area, the file protection code will be set in the Logical Status when FIB+LSN greater than FIE.

*) Note: The first sector requires a special treatment:
The data octads and the EOL octad should be skipped.
The other fields denote the sector and the IO Area for the first load operation.

IOD Lay-out (shown one word per line), at command:



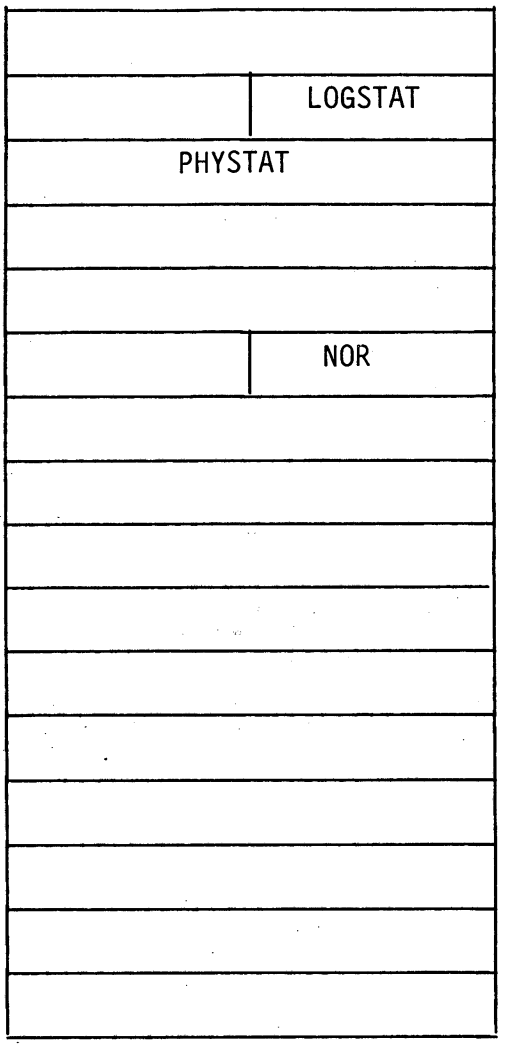
*) FXD/RMD/CMD

Bit	meaning
0	1=Fixed of RMD/CMD 0=Other
1	Reserved for hardware (must be zero)
2:7	NTC

Other disks

Bit	meaning
0	0=Flexible 1=MDD
1	0=Single 1=Double Density
2	0=PHILIPS 1=IBM Format
3	Claimed for extension
4:7	NTC (NR of tracks/set)

At Interrupt:



2.2.2.15 FORMAT PACK Command Code : '10'X
(Certain disk units only, see 2.2.8 and 2.2.9)

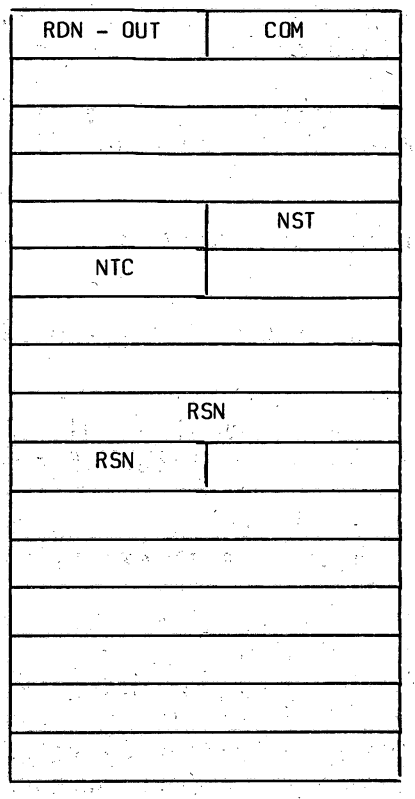
This command can be used to speed up formatting of a pack.
This command will write the gaps, the sector identifier and data blocks occurring on the disk unit, track by track.

The track on which this command should start is the track denoted by RSN (Real Sector Number) as indicated in the IOD.
The track on which this command ends is the last track as indicated by the access parameters NOC and NOH on the disk unit if no error occurs. If no error occurred, the field RRSN has no meaning. The command will also end if an error occurs.

The identifier is composed by hardware with a flag octad, indicating a non-defective track, the data field is composed by hardware. CA= 1 by writing 256 all ones octads. After a track has been written, the sector identifiers are checked with the previously written check octads.

In case an error occurs during the execution of the command the track on which the error occurred is the track denoted by the field RRSN (Return Real Sector Number) in the IOD. This makes it possible to continue if an error occurred.

IOD Lay-out (shown one word per line), at command:



Relative Device Number,
Command

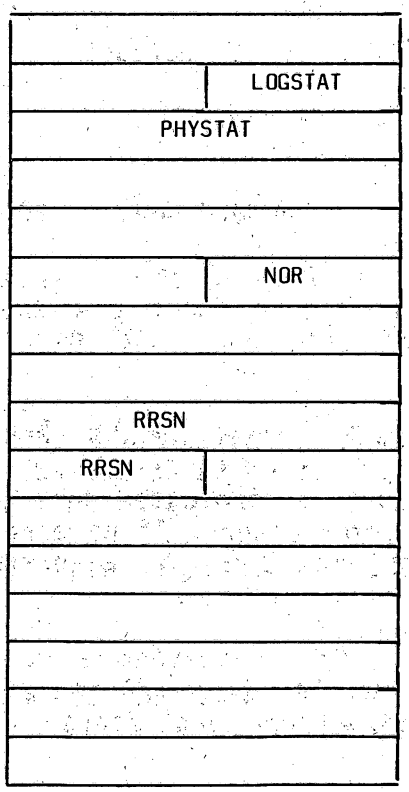
Number of Sectors per track

Mode; number of tracks/track set *)

Real Sector Number

*) FXD/RMD/CMD Bit	meaning	Other disks Bit	meaning
0	1=Fixed of RMD/CMD 0=Other	0	0=Flexible 1=MDD
1	Reserved for hardware (must be zero)	1	0=Single 1=Double Density
		2	0=PHILIPS 1=IBM Format
		3	Claimed for extension
2:7	NTC	4:7	NTC (NR of tracks/set)

At interrupt:



Logical Status

Physical Status

Number of Retries
(not for FXD/RMD)

Return Real Sector Number

CX

In an (indexed) disk file, data records are characterized by keys. To allow smooth retrieval of the Logical Sector Numbers of such data records, their keys are recorded in an index data set.
This index data set can be thought of as a list of all keys in an ascending order, each key accompanied by the logical block number of the corresponding data record.

To allow for smooth key look-up and ditto modifications in this list of keys, the list itself is organized in a very specific manner.

Indeed there is such a thing as a list of keys in ascending order. It is stored in a series of "BLOCKS" (called "LEVEL-0 BLOCKS").

As soon as there are more such blocks, (which usually is the case), a "HIGHER LEVEL" of blocks exists, listing all level-0 blocks, in ascending order of the highest keys contained in said level-0 blocks.

As soon as any such level contains more such blocks, a higher level exists to show the way in the lower level.

A block can contain up to 256 octads; it is always contained in one sector.
The precise layout of a block is specified later in this command description.

So, a certain key (and thus, implicitly, a piece of indexed data) can be found by searching the highest block level for a lower block that will show in more detail where the desired key is located, and by continuing this process through all levels until, at level-0, the pointer to the desired data record has been found. If no equal key is found, then the position of the next higher key is returned.
The command "SEARCH MULTIPLE INDEX" facilitates such searching.

Note: The command will be rejected if issued for a "SECTOR" of 128 octads.

Throughout the detailed description below, "BLOCK NUMBERS" are used.
A block with block number BN corresponds with the logical sector.

LSN = BN - 1.

Input data and output data may be given or returned in the IOD, in the IO area in the "Key Area" or in the "IO extension area". The latter two areas are detailed later in the description of this command.

- The IOD is found as usual.
- The IO Area is found as usual, via "IOAA" in the IOD.
  It has a length of 256 octads to hold a complete "block" of up to 256 octads.
- The key area is found via the field "key area address" in the IO extension area.
  For convenience of some implementations, a copy of the "key area address" is in the IOD. It has a length of KL+1 octads (KL from IOD).
- The IO Extension Area is found via field "IOEA" in the IOD.
  Its length is 56 octads.
  All addresses as mentioned above are protected according to the same scheme as for the address "IOAA"; for every address used, the appropriate length is taken into account.

Input data are:

. A key. This key is found in the "key Area"
. The block number of a highest level block (FBN from IOD).
. An indication if search should be continued through all levels, or that searching should consider the level of the "highest" block already to be zero. This indication is given by means of the field "Levels"in the "IO Extension Area":

- Levels = '00'X : "one level search".
- Levels = any other value: search until level = 0

Data to be returned are:

. The "Block Numbers" of all blocks, "passed" in the searching process.
  These numbers are returned into the IO Extension area.
  Space is reserved for 16 (24 bit) such block numbers.
  Each of these BN corresponds to a level, the first one containing the block number of the level-0 block.

. The complete contents of the block where the search ended.
  This field is recorded in the IO-Area. The exact position of the (equal or next higher) key within the block, to be returned in field "keypos" in the IO Extension Area.
  As a block can not be over 256 octads, the leading two octads of this field are always made zero.

. The number of (least significant) octads different from those in the next lower key (reflected in the field "key-diff" in the IO Extension Area).
  For precise explanation, see bottom of this command description.

. Status indication, possibly showing:

  "Search unsuccessful" (Logical Status= '02'X) e.g. because presented key too high

  Lay-out of the Extension Area:

```
      DECLARE
   1  IO - Extention Area                MODEL
           2  KEY-Area-Address           Pointer (24)
           2  Levels                     integer (8)
           2  Key-Diff                   integer (8)
           2  Key-Pos                    integer (24)
           2  Search-path-bn (0:15)      pointer (24)
```

All entities in the IO-Area have been explained above.

Lay-out of a block:

```
Declare
1   Index-Block                     Model
    2  Level-number                 integer (8)
    2  Index-Entries (1:N)
       3  Key-Diff-Length           integer (8)
       3  Key-Value                 character (Key-Diff-Length)
       3  Data                      integer (24)
    2  free-space
       3  termination-octad         integer (8) initial ('FF'X)
       3  not-relevant              integer (remaining-length)
```

In which:

Level-Number
: Has been explained above.

Key-Diff-Length
: Contains the number of characters by which this key differs from its predecessor (0 = Keys Equal)

Key-Value -
: Those characters by which this key differs from its predecessor. This gives a significant reduction in disk space, but it means that only those keys are recorded completely which, either appear at the beginning of their block, or differ already in the first character from their predecessor.

Data - This 24 bits integer is a Block Number indicating the appropriate next lower block or, from block level - 0, pointing to the appropriate sector in the data file itself.
(The translation "Block Number" to "Logical Sector Number" has been explained above).

TERMINATION-OCTAD -
: As explained above: A Key-Diff-Length field containing 'FF'X indicates the end of the block.

IOD Lay-out (shown one word per line), at command:

RDN - out	COM	Relative Device Number, Command
IOEA		IO area Extension Address (octad, real)
IOEA	NST	Number of sectors per track
NTC		Mode; nr of tracks/track set *)
	IOAA	IO Area Address (octad, real)
IOAA		
	FBN	First Block Number
FBN		
KA		Key Address (Octad, Real)
KA	FIB	File Begin (Real Sector Number)
FIB		
FIE		File End (Real Sector Number)
FIE	KL	Key Length (octads-1)

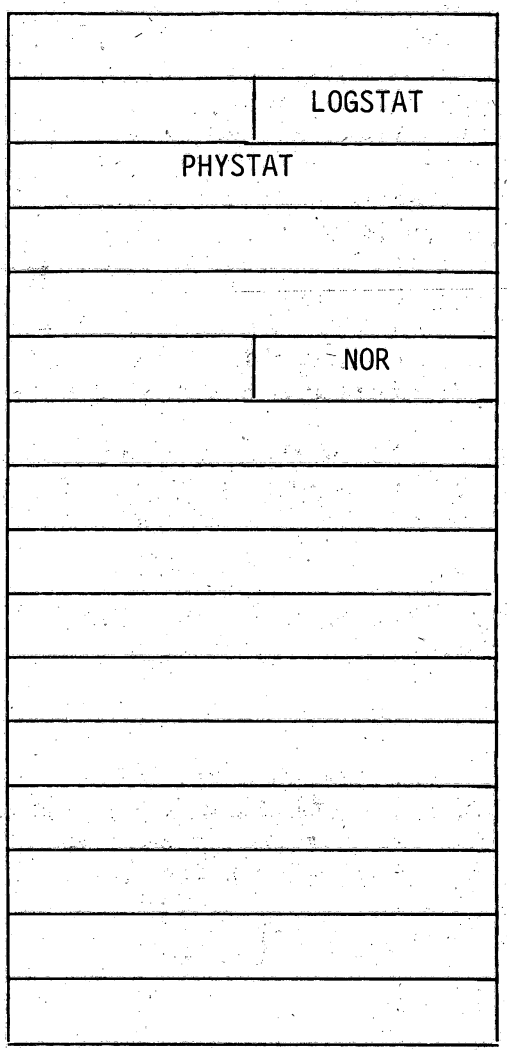
*) FXD/RMD/CMD

Bit	meaning
0	1=Fixed of RMD/CMD 0=Other
1	Reserved for hardware (must be zero)
2:7	NTC

Other disks

Bit	meaning
0	0=Flexible 1=MDD
1	0=Single 1=Double Density
2	0=PHILIPS 1=IBM Format
3	Claimed for extension
4:7	NTC (NR of tracks/set)

At Interrupt:



Logical Status

Physical Status

Number Of Retries
(not for FXD/RMD)

The instruction proceeds as follows:

1. The block, indicated by RSN (as in the IOD) is located.

2. The keys, appearing in this block and coded as described above ("Layout of a block") are compared with the key as presented in the Key Area.
   Note that the first key in a block is given completely, any further keys may be presented in the reduced manner as explained.
   Furthermore, the appropriate entry in the "Search-Path" (in the IO-Extension Area) is updated, reflecting the block number used.

3. As soon as an "Equal or High" has been found:

   (1) If "Levels" = 0, final reporting is done and the instruction is completed.
   (2) If the level of the last processed block = 0, final reporting is done and the instruction is completed.
   (3) If neither "Levels" nor the Level of the last block equals zero, the "Data" as given with the key for which "Equal or High" was found is used as a block number of the next block to be investigated, and process step "2" above is entered again.
   (4) As soon as "End Of Block" has been found:
   Final reporting is done and the instruction is completed. Note that the Logical Status indicates "SEARCH UNSUCCESSFULL".

4. "Final Reporting" includes:

   1) Returning the complete blocks just processed into the IO-Area.
   2) Returning into the IO extension area the octad number within the block where the "Equal or High" key or the "End Of Block character" was found.
   3) Returning a "Key-Diff" as explained below into the IO-Extension Area.

Explanation of the notion "Key-Diff":

Effective key:

What will be called an "Effective key" is a key that would have been recorded if no compression were applied (So, all Effective keys have a length KL + 1).
The effective key according to an entry in an index block can be found by replacing the "Key-Diff-Length" least significant octads of the previous effective key (if any) by the octads "Key value" as in the entry.

Key-Diff:

If there is no previous effective key (first recorded key already given key) then: no meaning.

If the effective key is equal to the specified key then: zero.
Else: The number of octads by which the previous effective key differs from the specified key.

(4) Normal conclusion of any IO command (e.g. providing status indications).

2.2.3 RECOVERY AND SERVICE COMMANDS

These commands will not occur in "NORMAL" SOFTWARE.

2.2.3.1 RECOVERY COMMANDS

These commands are necessary for recovery of seek errors, read errors.
IOD lay-out of all commands: see 'UNLOCK'
Note: The Physical and Logical Status octads are filled with zeroes except for "Return To Zero" and "Retry".

RETRY (FXD and RMD only) Command Code: '1D'X

The normal command which was last executed must be retried at the point where the error was detected.

Note: The Physical and logical status will be as for retried command.

SUPPRESS RETRY (flexible and MDD only) Command Code: '1D'X

From the moment this command was given, the hardware will not provide any recovery.

ENABLE RETRY (flexible and MDD only) Command Code: '1E'X

From the moment this command was given, the hardware will (again) provide all available recovery.

RETURN TO ZERO Command Code: '17'X

A recallibration is made: the actuator is sent slowly to track 0, with the last selected head. The seek error condition in the drive is reset.

The bits Unsafe 1, Unsafe 2, and NOT OPERABLE, in the physical status are filled in normally. All other bits in the physical and logical status are filled with zeroes.

POSITIVE OFFSET (FXD and RMD only) Command Code: '13'X

For the following command the actuator will be offset TOWARDS the spindle. It is not allowed to write in an offset position.
The offset position is reset with the next sector.

NEGATIVE OFFSET (FXD and RMD only) Command Code: '1C'X

For the following command the actuator will be offset from the spindle. It is not allowed to write in an offset position.
The offset position is reset with the next seek action.

DATA STROBE EARLY (FXD and RMD only) Command Code: '14'X

For the following command the PLL data-separator is forced to strobe the data earlier than nominal.
The strobe is set to normal with the next seek action.

DATA STROBE LATE (FXD and RMD only) Command Code: '15'X

For the following command the PLL data-separator is forced to strobe the data later than nominal. The strobe is set to normal with the next seek action.

2.2.3.2 SERVICE COMMANDS

These commands are an aid to diagnose error.

READ IDENTIFIER Command Code: '12'X

This command provides for reading of identifiers of the track, that is indicated by the RSN-field in the IOD. Reading starts with an arbitrary sector.

Reading is continued with the next sector (Identifer) until the total of read identifiers is greater than the number of sectors per track or the IO-Area is completely filled.

IOD lay-out: see 'READ DATA'

Note: This command may only be given to formattted tracks.
8 octads are transferred.
They contain the identifier and the CRC octads.

FXD/RMD: Software Recovery;
Other : Control Unit Recovery.

2.2.4 PHYSICAL STATUS INFORMATION

Significance of the Physical Status:

OCTAD 0

Bit 0 - UNSAFE 1
FXD/RMD : If the drive indicates "seek error" during command execution.
Other : Not used.
FXD/RMD : Software Recovery;
Other : Not Applicable

Bit 1 - not used.

Bit 2 - DATA PART TIME OUT

This bit is set if a data block does not follow the corresponding sector identifier within a certain time limit.

FXD/RMD: Software Recovery;
Other : Control Unit Recovery.

Bit 3 - UNSAFE 2

FXD/RMD : This bit is set if during command execution a disk "fault" condition occurs.
Other : Not used.

Recovery : None

Note: It is possible that during read actions, data on the track is damaged or that during write actions, data on more than one track has been written.

Bit 4 - HAS BEEN NOT READY

Only for flexible disk, mini fixed disk an CDC drives. This bit is set when the drive goes from not ready to ready. The bit can be reset by the "TOPER" command only.

Bit 5 - READ DATA ERROR

This bit is set if a data block is read with errors or an error occurred in the data block during a check-read (where applicable).

FXD/RMD: Software recovery;
Other : Control Unit recovery.

Bit 6 - NOT OPERABLE

This bit is set before command execution if one of the following conditions is fulfilled:

- If drive indicates "Unit Not Ready"
- If drive can not be selected (FXD/RMD only)

This bit will also be set during command execution if the "Stop" button on the disk operator panel is activated (RMD only).
Whatever the condition was, and whichever command was given, this situation will always lead to execution of the command "Unlock".

Recovery: The operator should be warned (software)

Bit 7 - NO IDENTIFIER DETECTION

This bit is set when it is impossible to detect at least one identifier on the selected track.

FXD/RMD: Software recovery;
Other : Control Unit recovery.

OCTAD 1

Bit 0 - Not used.

Bit 1 - Not used.

Bit 2 - FLAG ERROR

This bit is set if:
- an alternate track is found instead of a primary
- a primary or defective track is found instead of an alternate
- The bit pattern indicates no primary, no alternate or no defective track at all.

FXD/RMD : Software recovery;
Other: Control unit recovery.

Bit 3 - NO CORRECT HEAD NUMBER OR TRACK SET NUMBER

This bit is set when during read or write actions a check in the identifiers of the selected track results in the detection of only wrong head and/or track set numbers.

FXD/RMD : Software recovery;
Other: Control unit recovery.

Bit 4 - NO CORRECT SECTOR NUMBER

This bit is set when during read or write actions a check in the identifiers of the selected track results in the detection of only wrong sector numbers.

FXD/RMD : Software recovery;
Other: Control unit recovery.

Bit 5 - WRITE PROTECT (FLEXIBLE DISK ONLY)

This bit is set if write protection for a flexible disk is detected.
Recovery: none. (operator should be warned)

Bit 6 - IDENTIFIER ERROR

This is set if the identifier is found but reading of the contents is impossible because of read errors or general format errors.
This condition can also occur during execution of format commands.

FXD/RMD : Software recovery;
Other: Control unit recovery.

Bit 7 - THROUGHPUT ERROR

This is set when the transport of data to or from main store could not follow the speed of the disk.
FXD/RMD : Software recovery;
Other: Control unit recovery.

Note 1: No error recovery will be performed during commands "Unlock" and "Toper".

Note 2: (FXD/RMD only) during the commands "Format Track", "Format Defective Track and "Format Alternate Track", error recovery will only be performed in case of the Physical errors "Unsafe 1" or "No correct head number of track set number".

2.2.5 LOGICAL STATUS INFORMATION:

Value '00'X - NORMALLY ENDED - standard meaning

Value '02'X - SEARCH UNSUCCESSFUL
This value is set if, during the execution of one of the search commands the indicated search action is not successful.

Value '03'X - IRRECOVERABLE ERROR - Augmented Standard Meaning. Not for FXD/RMD.
This value is set when a not recoverable error is detected or when the total number of retries of control unit and device together exceeds the value of 32 or when the drive is inoperable (not for commands "Toper" or "Unlock").

Value '04'X - FILE PROTECTION
The value is set when the Real Sector Number (RSN) or one of the following involved sectors exceeds the file parameters (FIB and FIE) specified in the IOD. File protection is only checked for the commands "Program Load" and "Search Multiple Index".

Value '06'X - DEVICE BUSY - standard meaning
This value is set if the maximum number of I/O operations that may be outstanding for a device is exceeded.

Value '07'X - RDN NOT PRESENT
The condition will be given if a CIO start instruction was performed with a non existing Relative Device Number in the IOD.

Value '09'X - MEMORY PROTECTION
This value is set when one of the involved IO Area's exceeds the memory boundaries (PAB and PAE) specified in the IOD. The check will be done before actual command execution. Memory protection will only be checked for the command "Program Load".

Value '12'X - DELETED DATA ADDRESS MARK
Not for FXD/RMD/MDD
This value is set whenever a read command for flexible disk encountered a sector in which the "Deleted Data" mark was present

Value '20'X - COMMAND REJECTED
This condition indicates that the specified command code does not exist for the peripheral designated in the RDN-out field of the IOD, or is not allowed for the control unit at this moment.

2.2.6 (T.B.S)

2.2.7 INTERRUPTS

The "Peripheral Attention Interrupt" will be given when the peripheral changes state from Inoperable to Operable.

2.2.8 PARTICULARS ON 5 1/4 inch FLEXIBLE DISK UNITS

2.2.8.1 COMMANDS

The following commands are supported:

GENERAL COMMANDS (see 2.2.1)

'80'X Test Control Unit
'81'X Terminate
'82'X IPL
'83'X Read Identification

NORMAL DISK COMMANDS (SEE 2.2.2)

'00'X Read Data
'01'X Write Data
'02'X Search Key Equal
'03'X Search Key Equal with Data Return
'04'X Search Key Equal High
'05'X Search Key Equal High with Data Return
'06'X Format Track
'09'X Unlock
'0A'X Toper
'0B'X Indicate Access Parameters
'0C'X Program Load
'0E'X Write Deleted Data Address Mark
'0F'X Search Multiple Index

ERROR RECOVERY (SEE 2.2.3.1)

'17'X Return to Zero
'1D'X Disable Retry
'1E'X Enable Retry

SERVICE COMMANDS (SEE 2.2.3.2)

'12'X Read Identifier (n.b. only one identifier is possible)

The following features are not supported:

Data chaining
Command chaining
Pending CIO for any device

The following features are not supported (Action: Command reject)

'07'X Format Defective Track
'08'X Format Alternative Track
'10'X Format Pack
'13'X Positive Offset
'14'X Data Strobe Early
'15'X Data Strobe Late
'1A'X Correct and Continue
'1C'X Negative Offset
'1F'X Read Diagnostic

2.2.8.2 GENERAL

A large variety of disk types can be connected to the controller. The properties of this disk drives must be given by means of the IAP (Indicate Access Parameters) command. In order to make IPL possible from any device without first giving an IAP-command the default values are chosen such, that even the most restricted drive fulfilling SA450 specifications can be used.
The various fields of the commands are described below.

2.2.8.2.1 NOC - Number Of Cylinders

This field specifies the number of cylinders on the connected disks. The default value is 255 ('00FF'X) to be able to IPL form any cylinder.

2.2.8.2.2 NOH - Number Of Heads

This field specifies the number of heads. The field is also present in any IOD, so IPL is possible without first giving an IAP comamnd. The default value is 2.

2.2.8.2.3 SRWCC - Start Reduced Write Current Cylinder number

This field specifies in this case the head load time, that is the time between loading the head and actually reading. This is drive dependant. All even figures between 2 and 254 are allowed. Default is 32 msec. For drives with 250KB transferrate the actual time will be X*32msec. Default is 15 (480 msec).

2.2.8.2.4 SWPCC - Start Write Precompensation Cylinder number

This field specifies in this case the head unload time, that is the time between the end of the execution of a read or write command and the unloading of the head (system dependant). All values X between 1 and 15 are allowed. The actual time will be X*16 msec. Default is 15 (240 msec).

2.2.8.2.5 ECCM - Maximum ECC length

This field is not used.

2.2.8.2.6 INTERL - Interleave factor

This field specifies the interleave (or skip-) factor for the sectors on a track. An interleave factor X means that it will take X revolutions to read a whole track. For optimal performance value 2 must be used. Only 1 (no interleave) or 2 is allowed. Default is 2.

The field INTERL will only be used for the FORMAT commands.

2.2.8.2.7 STEP - Step rate code

This field specifies the step rate code. Its meaning is the following:

HEX value	250KB Drive	500KB Drive
0	32 msec	16 msec
1	30 msec	15 msec
2	28 msec	14 msec
3	26 msec	13 msec
.	.	.
.	.	.
.	.	.
F	2 msec	1 msec

For some disk units which are known some figures are given below:

Type of disk unit	3114	3116
Capacity (roughly), Mocts	1	2
Number of sectors per track	16	32
Number of tracks per track set	2	2
Number of track sets	80	80
Number of heads per surface	1	1
Number of data surfaces	2	2
Fastest step rate code	TBS	TBS
Head Load Time	30 msec	30 msec

A track set is a collection of tracks that can be used without arm (head) movement.
The track organisation is a sectorized one with a layout which is given by the access parameters.
Sector 00 is positioned after index on the track.
Track assignment is as follows
Primary tracks on track set 000 thru NOC-2
Service tracks on track set NOC-1
The service tracks have no alternate possibility. They can have errors but will have at least one error-free sector.
Recording mode:
On disk : MFM, except track 0 (FM)
At Interface : MFM, except track 0 (FM)

2.2.8.3 SECTOR LAYOUT

The layout of a sector is standard IBM single and double density format

2.2.8.4 SECTOR POSITION CALCULATION

This is done by the control unit

. TS-NR (track set number),
. HD-NR (head number) and
. SC-NR (sector number within track)
  can be derived from
. RSN (real sector number)
  By breaking down the formula:
  RSN = N-O-H*N-O-S*TS-NR + N-O-S*HD-NR + SC-NR.

In which N-O-H is the number of tracks per trackset ("number of heads") as specified in the table in section 2.2.8.2 and in which N-O-S is the number of sectors per track.

2.2.9 PARTICULARS ON FIXED DISK UNITS 5 1/4 INCH ON WDE

2.2.9.1 COMMANDS

The following commands are supported:

GENERAL COMMANDS (see 2.2.1)

'80'X Test control unit
'81'X Terminate
'82'X IPL
'83'X Read identification

NORMAL DISK COMMANDS (see 2.2.2)

'00'X Read Data
'01'X Write Data
'02'X Search Key equal
'03'X Search Key equal with Data Return
'04'X Search Key High
'05'X Search Key High with Data Return
'06'X Format Track
'07'X Format Defective Track
'08'X Format Alternate Track
'0A'X Toper
'0B'X Indicate Access Parameters
'0C'X Program load
'0F'X Search Multiple Index
'10'X Format pack

ERROR RECOVERY (SEE 2.2.3.1)

'17'X Return to Zero
'1D'X Disable Retry
'1E'X Enable Retry

SERVICE COMMANDS (see 2.2.3.2)

'12'X Read Identifier (note that only one identifier will be transmitted)

The following features are not supported:

Data Chaining
Command Chaining
Pending CIO for any device.

The following commands are not supported (action: Command reject):

'0E'X Write deleted data address mark
'0A'X Correct and continue
'13'X Positive offset
'14'X Data strobe early
'15'X Data strobe late
'1C'X Negative offset
'1F'X Read diagnostic

The following command are not supported (action: NO-OP):

'09'X Unlock

2.2.9.2 GENERAL

Onto the control unit 3 drives with exactly the same characteristics may be connected. A large variety of disk types can be connected to the control unit. The properties of these disk drives must be given by means of the IAP (Indicate Access Parameters) command. In order to make IPL possible from any device without first giving an IAP-command the default values are chosen such, that even the most restricted drive fulfilling ST506 specifications can be used.

The various fields of the commands are described below.

2.2.9.2.1 NOC - Number of cylinders

This field specifies the number of cylinders on the connected disks. The default value is 306 ('0132'X). This field is only used for the command 'Format pack'.

2.2.9.2.2 NOH - Number of heads.

This field specifies the number of heads. The field is also present in any IOD, so IPL is possible without first giving an IAP command. The fefault value is 4.

2.2.9.2.3 SRWCC - Start reduced write current cylinder number.

This field specifies the cylinder number from which the write current must be reduced. As the IPL command does not write, it does not influence the execution. The default value is 128 ('0080'X).

2.2.9.2.4 SWPCC - Start write precompensation cylinder number

This field specifies the cylinder number from which the write precompendation must be applied. As the IPL command does not write, it does not influence the execution. The default value is 0. This field is ignored, always default.

2.2.9.2.5 ECCM - Maximum ECC length

This field specifies the maximum length of the error to be corrected. The default value is its maximum, 11. So it is possible to correct errors with a burst of 11 at most. This field is ignored, always default.

2.2.9.2.6 INTERL - Interleave factor

This field specifies the interleave (or skip-) factor for the sectors on a track. An interleave factor X means that it will take X revolutions to read a whole track. For optimal performance the default value 3 must be used.
This field is ignored, always default.

2.2.9.2.7 STEP - Step rate code

This field specifies the step rate code during recallibrate. Its meaning is the following:

HEX value	Meaning
'0'X	32 Msec.
'1'X	30
'2'X	28
'3'X	26
'4'X	24
'5'X	22
'6'X	20
'7'X	18
'8'X	16
'9'X	14
'A'X	12
'B'X	10
'C'X	8
'D'X	6
'E'X	4 Default.
'F'X	2

For some disk units which are qualified some figures are given below:

Type of disk unit	RODIME202	ST412	RODIME202E	204E
Capacity (roughly), MOCTS	10	10	20	40
Number of sectors per track	32	32	32	32 always
Number of tracks per track set	4	4	4	8
Number of track sets	320	306	640	640
Number of heads per surface	1	1	1	1
Number of data surfaces	4	4	4	8
Step rate code	'OE'X **	'OE'X	'OE'X	'OE'X
Number of alternates (advise)	6	6	6	6

* The number of track sets (cylinders). It is possible (e.g. for dimming reasons) to use less cylinders.
** By cutting a link in the drive, else 'OF'X.

A track set is a collection of tracks that can be used without arm (head) movement.

The track organisation is a sectorized one with a layout which is given by the access parameters.

Sector 00 is positioned after index on the track.

Track assignment is as follows (RODIME and SEAGATE):

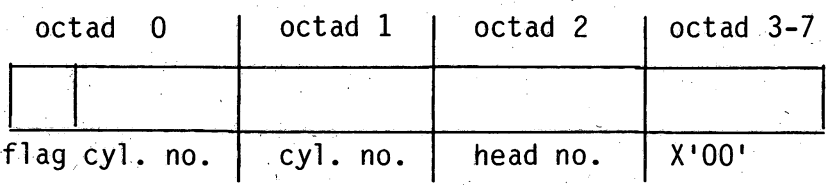
Primary tracks on track set 000 THRU NOC-8
Alternate tracks on track set NOC-2, -3, -4, -5, -6, -7
Service tracks on track set NOC-1

The service tracks have no alternate possibility. They can have errors but will have at least one error-free sector.

Recording mode:
on disk : MFM
at interface : MFM (between control unit and disk).

2.2.9.3 SECTOR LAYOUT

The layout of a sector is determined by the control unit. This means that an identifier read with read identifier has the following layout:



Flag: 00 = normal
01 = defective
10 = alternate.

2.2.9.4 SECTOR POSITION CALCULATION

This is done by the controller.

. TS-NR (Track set number)
. HD-NR (Head number) and
. SC-NR (Sector number within track) can be derived from
. RSN (Real sector number) by breaking down the formula:

RSN = N-O-H*N-O-S*TS-NR + N-O-S*HD-NR + SC-NR.

In which N-O-H is the number of tracks per trackset ("Number of heads") as specified in the table in section 2.2.9.2 and in which N-O-S is the number of sectors per track.

2.3 THE HARDWARE OF THE DFA

In the block diagram the following functional parts can be seen:

1. Microprocessor
2. Local memory
3. DMA
4. UPL-bus interface
5. Disk drive interface
6. DTI interface
7. Control part

2.3.1 MICROPROCESSOR

The microprocessor is a 8085, which is using a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus, which gives a 16 bit address but after latching the databus..
The microprocessor executes the micro instructions stored in the EPROM.
Further on he selects the modes of the DMA controller and gives control of the data address bus to the DMA.
The 8085 has also 4 vectored interrupts inputs which are used by the HDC (Hard Disk Controller), FDC (Flexible disk Controller) and the DMA to interrupt the processor.
The serial In/Serial Out port of the processor are used by the DTI (Diagnostic Test Interface).

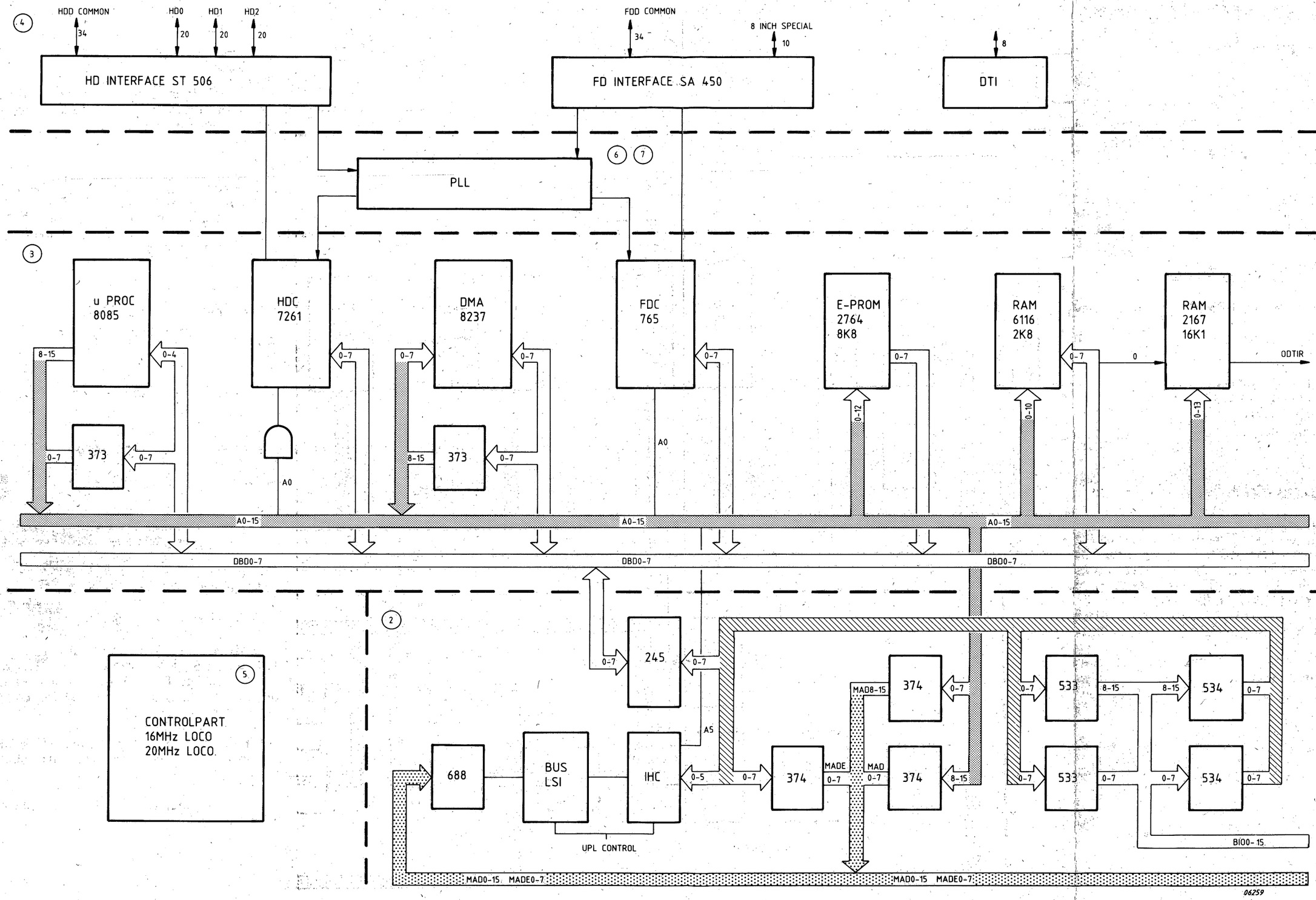


Figure 2.1 BLOCK DIAGRAM WDE

2.3.2 LOCAL MEMORY

The local memory consists of 3 parts

1. EPROM - the 8K8 EPROM contains the complete firmware for the WDE.
2. RAM - The 2K8 RAM is used for the IO administration and data buffer.
3. DTI-RAM - The 16K1 RAM is used to set a trap on the diagnostic test interface

2.3.3 DMA

The DMA (Direct Memory Access) is used to control the data transfer between controller and local memory and also the data transfer between local memory and main memory. Control of the DMA is handles by the processor.

2.3.4 UPL-BUS INTERFACE

The UPL-bus interface consists of the following functional areas:

1. BUSLSI
2. IHC (Interrupt Handler Chip)
3. MAD/MADE Registers
4. BION Registers

In this system, the CU only recognises two commands give by the CPU.

Those being: - CIO start (Command Input/Output)
- SST (Send Status)

The command are sent via the address lines which form a part of the UPL-bus. The address lines also contain the Control Unit number, which is compared with a hardware address (slot dependable - UPL 2), if the comparison is equal then the BUSLSI devices makes signal STARTF high.

The BUSLSI device is connected in 'CU' mode', and its function is to control the handshaking procedure on the system bus.

Data to and from the CU goes via the bi-directional datalines BIO- 00-15N. Internally there are two data busses DBD0-7 and DB0-7 connected to each other via a transceiver. The interface between DB0-7 and the BIO 000-15N lines is done via registers. There are two registers for input and two for output to convert the 8 bit internal bus to the 16 data bit system bus.

Addressing of the main memory uses the address lines MAD00-15 and MADE 0-7, coming from the MAD/MADE Registers. The address is composed out of the 16 internal address bits and the 8 internal data bits.

The IHC (Interrupt Handler Chip) can give a interrupt to the CPU via the BCI line (Binary Coded Interrupt) on the system bus.

2.3.5 DISK DRIVE INTERFACE

This part takes care of the data transport between the connected disk drives and the local memory.
For as well the hard disk as for the flexible disk part there is a controller chip to perform the proper operation to the drives. For the hard disk part this is the HDC (Hard Disk Controller) and for the flexible disk part this is the FDC (Flexible Disk Controller). These controllers are with the proper driver/ receivers HDI and FDI connected to the corresponding interface.

The PLL logic is common for the hard and flexible disk operation. As only one data transfer from drive to local memory takes place at a time the PLL-logic can be switched to the rigth one.

The PLL (Phase Locked Loop) Logic makes sure that the bit pulses of the CU stay in phase with the serial data pulses from the disk drives.

2.3.6 DTI-INTERFACE

The Diagnostic Test Interface (DTI) has a direct connection with the processor. This interface is used to read and write in local memory. Beside that there is the possibility to built in a trap to stop processing at a certain address, this is done via the DTI-RAM.

2.3.7 CONTROL PART

The control part consists of additional logic such as FPLA's, addressable latches and so on, to control the proper operation of all the operation modes and selection of the main memory parts by the micro processor.

2.3.8 DATA FLOW

2.3.8.1 WRITE DATA TO DISK

The data is coming from the system bus and latched into two latches, one for the least significant octad and one for the most significant octad.
The information of the latches is written into the RAM one by one.
If a complete sector is in RAM the data will be transfered to the disk controller (Flex. disk or hard disk controller).
From there the data is sent serial onto the disk interface (Flex. or hard disk interface).
The internal addressing will be done under controll of the DMA.

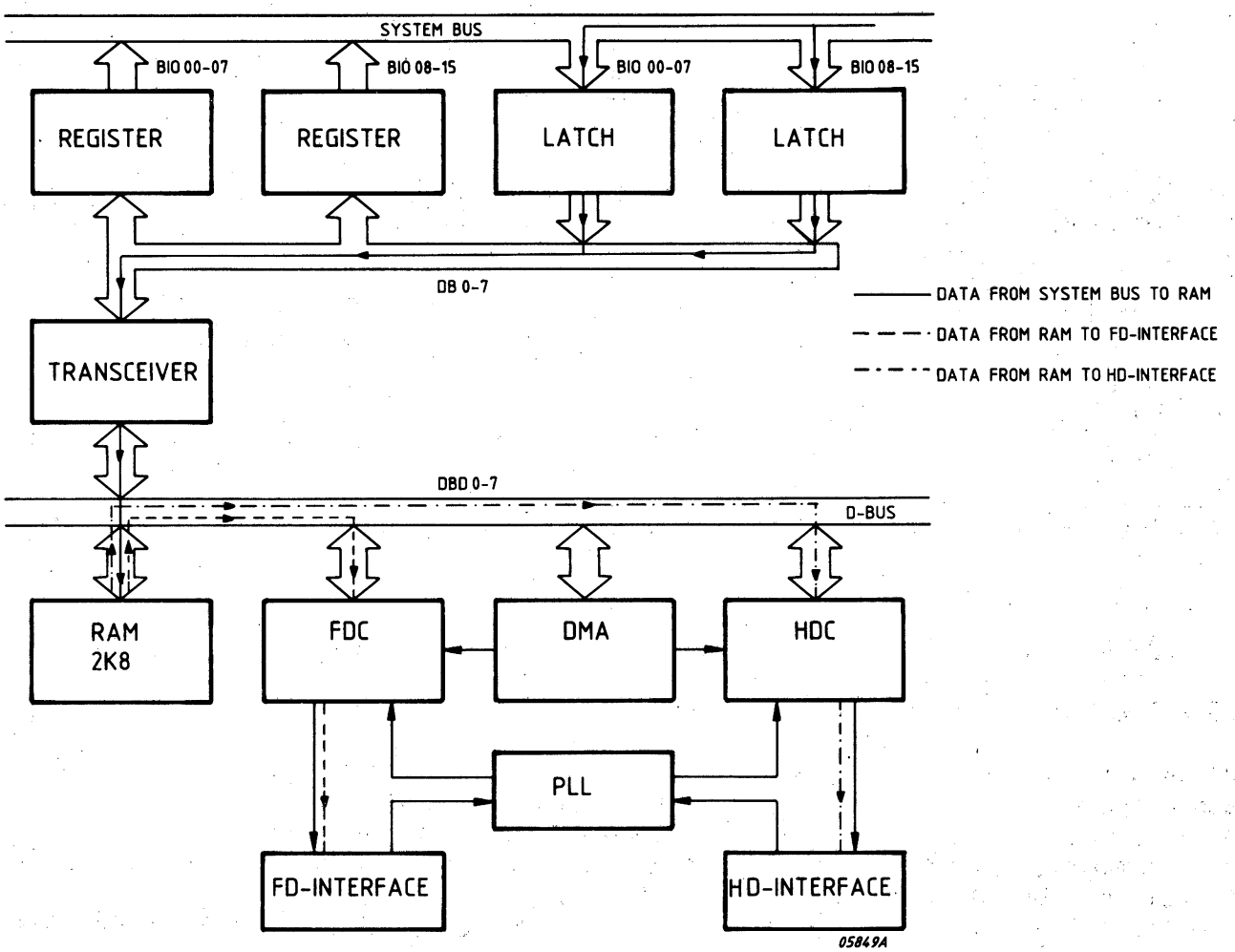


Figure 2.2 WRITE DATA

2.3.8.2 READ DATA FROM DISK

The serial data is coming from the disk interface (Flex. disk or hard disk) and sent via the PLL (Phase Lokced Loop) to the disk controller (Flex. disk or hard disk controller).

Then the data (bytes) is transfered to the RAM, until a complete sector is stored in RAM. At that moment the RAM will be read and data is put in the registers via the transceiver.

There are two registers, one for the least significant octad and one for the most significant octad.
When both registers are filled the complete word is put onto the system bus.
The internal addressing will be done under control of the DMA.

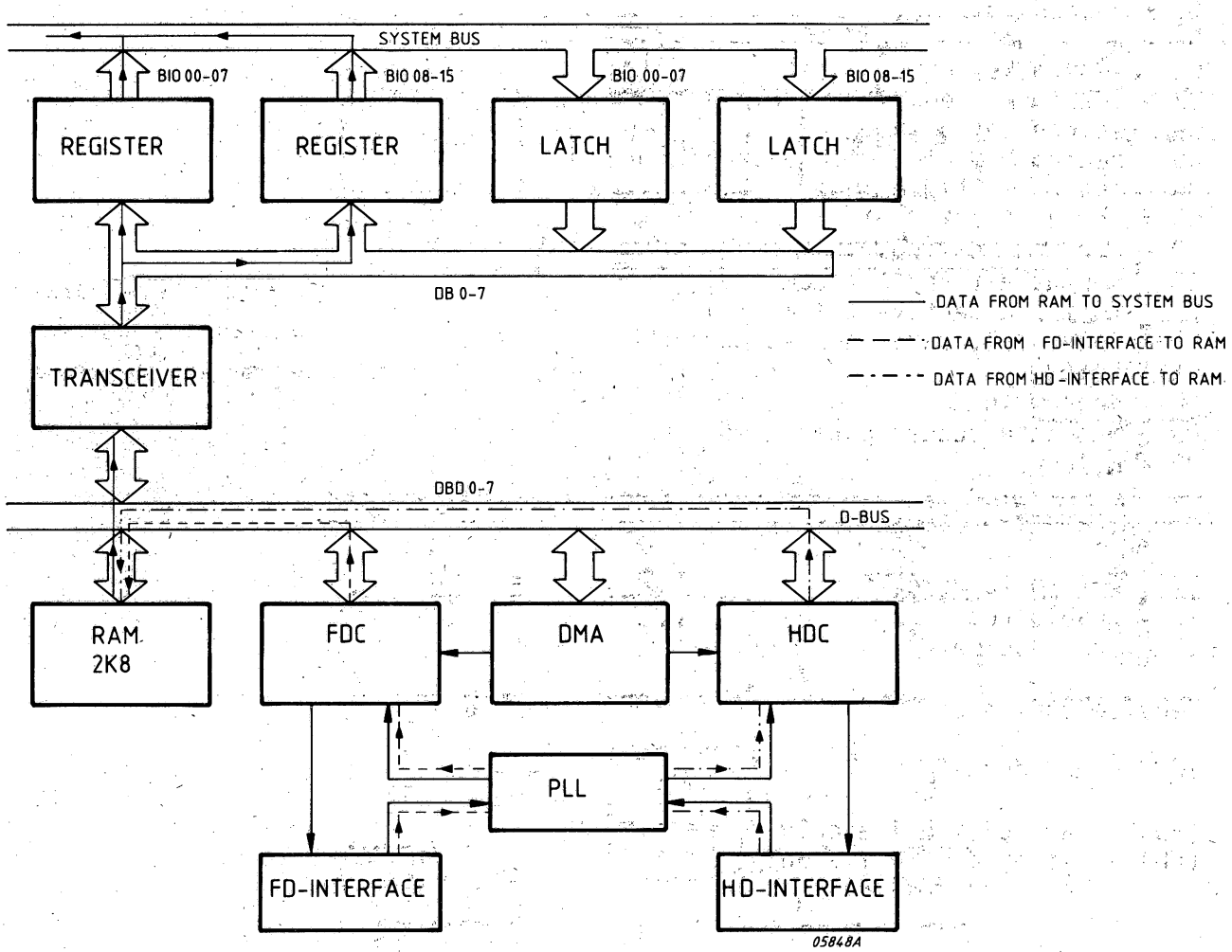


Figure 2.3 READ DATA

2.4 MICRO-PROGRAM OF THE DFP

2.4.1 HSI-COMMANDS

At HSI level the following commands are provided.

1. General Commands

   80 - test CU
   81 - terminate
   82 - IPL
   83 - read identification

2. Normal disk commands

   00 - read data
   01 - write data
   02 - search key equal
   03 - search key equal with the data return
   04 - search key high
   05 - search key high with data return
   0F - search multiple index
   06 - format track
   10 - format pack (HD)
   08 - format alternate track (HD)
   07 - format detective track (HD)
   0E - write del, data address mark (FD)
   0A - toper
   0C - prgram load
   0B - indicate access parameters
   09 - unlock

3. Error recovery commands

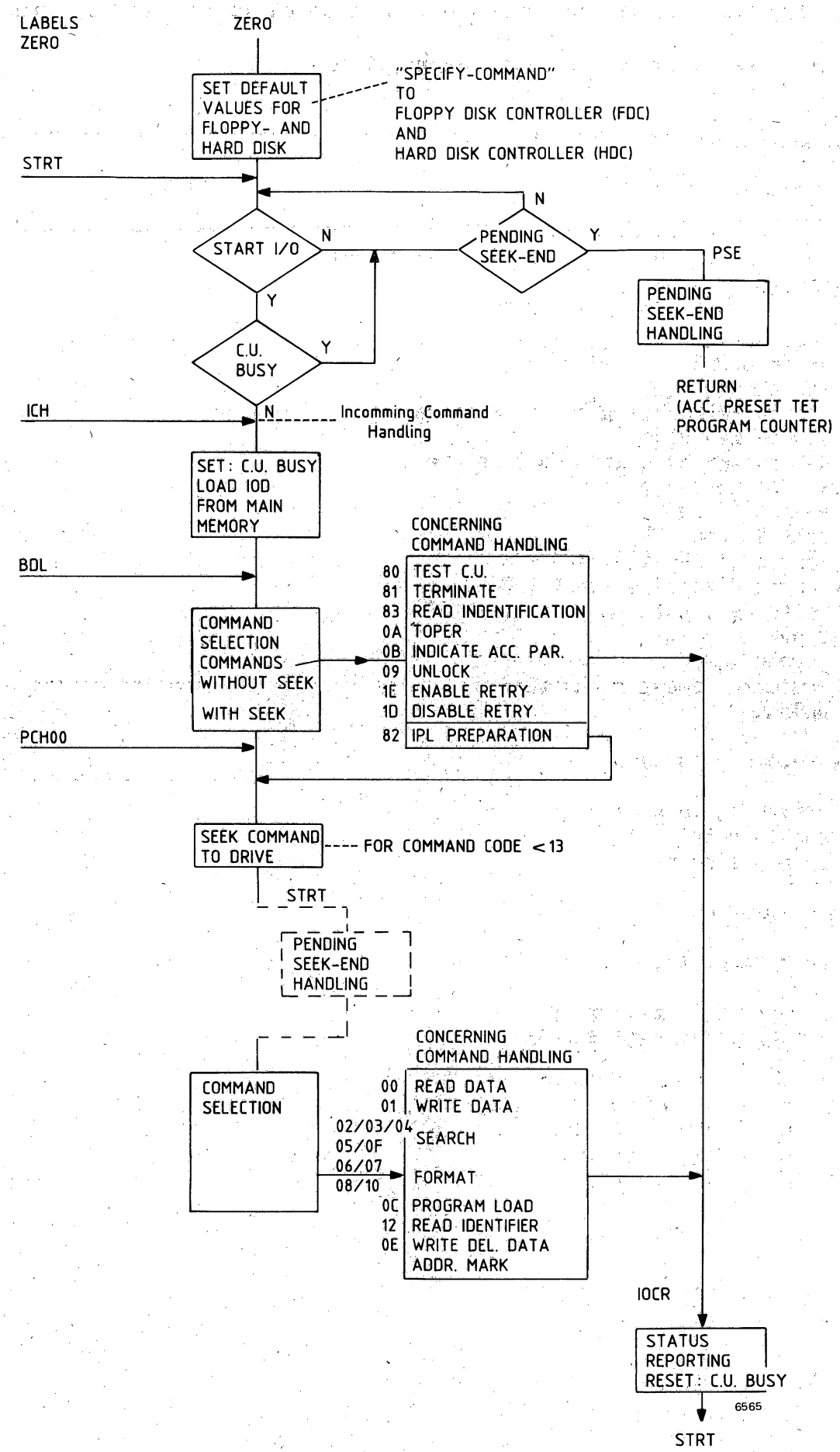
   17 - return to zero
   1E - enable retry
   1D - suppress retry

4. Service commands

   12 - read identifier

   (HD) = Hard Disk drive only
   (FD) = Floppy disk drive only

2.4.2 GENERAL FLOW OF THE MICROPROGRAM



2.4.3 LOGICAL AND PHYSICAL STATUS TABLE

Below a table of logical and physical status which is returned by this control unit.

Logical status table

CODE		DESCRIPTION
HEX	DEC	
2	2	Key not found/search unsuccessfull
3	3	Irrecoverable error
4	4	File - protection
7	7	RDN too high
9	9	Memory protection
0C	12	Deleted data address mark
20	32	Command rejected

Physical status table

CODE (HEX)		
PSO	PSI	
00	01	Throughput error/overrun
00	02	CRC identifier
00	04	Write protect
00	08	Wrong sector number
00	10	Wrong head/cyl. number
00	20	Flag error
00	40	
00	80	
01	00	No identifier found
02	00	Not operable
04	00	ECC/CRC error data field
08	00	HBNR (Has Been Not Ready)
10	00	Drive fault
20	00	Data parttime out
40	00	Ready change
80	00	LCN to high compared with NOC

3 DETAILED DESCRIPTION

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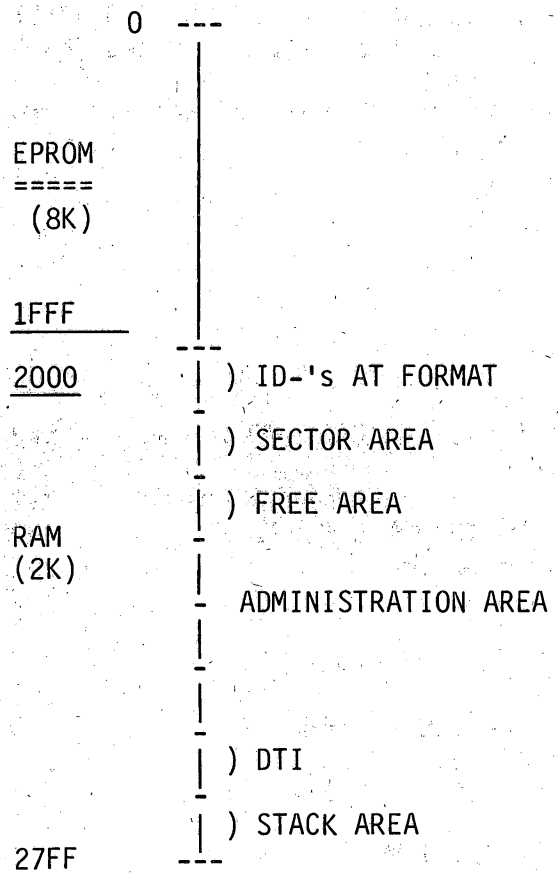
3 DETAILED DESCRIPTION

3.1 RELATION HARDWARE TO SOFTWARE

3.1.1 GENERAL

The main purpose of this control unit is to execute the HSI-commands as listed 2.4.1.
The execution of these HSI-commands is performed by the microprocessor on this board where its firmware is located in an EPROM.
Intermediate results are stored in a local memory.
The address location of EPROM and RAM is as given below.



The microprocessor system operates in the NON memory mapped I/O mode for easy connection of the DMA, HDC and FDC chips.
The I/O port accesses (using INPUT and OUTPUT instructions) will control the hardware such as:

- set/reset of static signals
- selective generated pulses
- read out of some hardware status signals
- load/readout of DMA, HDC and FDC.

In the Hardware description 3.2 (part 3.2.2 Control part) are tables given of all IO-addresses used.

Most of the HSI-commands result into an action to the Hard Disk or FLoppy diskdrive. This means that a number of actions to DMA, HDC or FDC are necessary.
As far as it the HDC or FDC concern we have a command field (COMD till COMD+8) and a result field (RESD till RESD+7) to sent the command bytes to the concerning controller and to receive the result bytes.
Part 3.1.3 gives the HDC commands used and a layout of the command and result field.
The same is given in part 3.1.4 for the FDC.

3.1.2 H.S.I. COMMANDS AND STATUS INFO

See chapter 2.

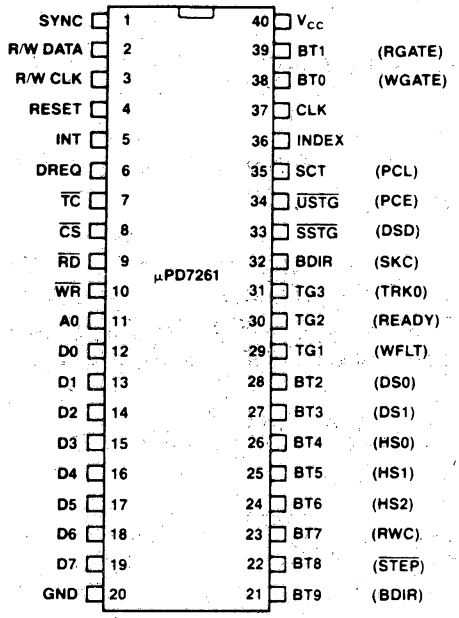
2.4.1 HSI COMMANDS

2.4.3 STATUS INFO

3.1.3 HDC (HARD DISK CONTROLLER 7261)

3.1.3.1 PIN CONFIGURATION

Pin Configuration



Note: Signals shown in parentheses are used when the μPD7261 is in the floppy-like mode.

Pin Identification

Pin No.	Pin Name	I/O	Function
4	RESET	I	Reset input. When high, it forces the device into an idle state. The device remains idle until a command is issued by the system.
5	INT	O	Interrupt request to the system, set high for request.
6	DREQ	O	DMA request. Normally low, set high to request a transfer of data between the disk controller and memory.
7	$\overline{TC}$	I	This is used as a terminal count input during DMA.
8	$\overline{CS}$	I	Chip select. When low, it enables reading from or writing into the register selected by A0.
9	$\overline{RD}$	I	Read strobe. When low, selected register contents are read.
10	$\overline{WR}$	I	Write strobe. When low, data is written into the selected register.
11	A0	I	Register select input, to be connected to a non-multiplexed address bus line. When high, the command status register is selected; when low, the data buffer is selected.
12-19	D0–D7	I/O	Data bus port, to be connected to data bus.
20	GND	P.S.	Ground.
36	INDEX	I	This signal indicates the beginning of sector zero.
37	CLOCK	I	External clock input, used as timing clock for the on-chip processor.
40	V_{CC}	P.S.	+5V power supply.

Disk Interface Pins

Pin No.	Pin Name
1	PLO Lock Read Clock Enable
2	Read Write Data
3	Read Clock | Write Clock
21	Direction In
22	Step Pulse
23	Reduced Write Current
24	Head Select 2^2
25	Head Select 2^1
26	Head Select 2^0
27	Drive Select 2^1
28	Drive Select 2^0
29	Write Fault
30	Ready
31	Track 000
32	Seek Complete
33	Drive Selected
34	Precomp Late
35	Precomp Early
36	Index
38	Write Gate
39	Read Gate

3.1.3.2 HDC-COMMANDS USED

From the 15 available commands the ones listed below are used by the control unit.

Used HDC commands

1. RECALIBRATE
2. SEEK
3. WRITE FORMAT
4. READ ID
5. READ DATA
6. WRITE DATA
7. SENSE INTERRUPT STATUS
8. SPECIFY
9. SENSE UNIT STATUS
10. DETECT ERROR

There are 4 auxiliary commands where the following 3 are used.

3.1.3.3 USED AUXILIARY COMMANDS

1. CHIP RESET
2. HALT SENSE INTERRUPT STATUS REQUEST
3. CLEAR COMMAND END BIT.

3.1.3.4 HD-COMMAND LAYOUT (MICRO-PROGRAM)

COMMAND-	READ WRITE	READ ID	RECAL	SEEK	FORMAT	SPECIFY	SENSE INT. STAT	DETECT ERROR	SENSE UNIT STAT
COMD	PHN	PHN			PHN	MODE			
COMD+1	LCNH	SCNT		LCHN	SCNT	DTLH			
COMD+2	LCNL			LCNL	DPAT	DTLL			
COMD+3	LHN				GPL1	ETN			
COMD+4	LSN				GPL3	ESN			
COMD+5	SCNT					GPL2			
COMD+6						RWNCH			
COMD+7	BX,FXH	9xH	5xH	6xH	7xH	RWCL	1xH	4xH	
COMD+8									

Note: COMD+7
Example : 9 x H
9 = command code READ IO
X = Drive no.
H = HEX.

Mnemonic Definitions

EADH	Error Address, High Byte
EADL	Error Address, Low Byte
EPT1	Error Pattern, Byte One
EPT2	Error Pattern, Byte Two
EPT3	Error Pattern, Byte Three
PCNH	Physical Cylinder Number, High Byte
PCNL	Physical Cylinder Number, Low Byte
PHN	Physical Head Number
PSN	Physical Sector Number
SCNT	Sector Count
DPAT	Data Pattern
GPL1	Gap Length One
GPL3	Gap Length Three
EST	Error Status Byte
FLAG	Flag Byte
LCNH	Logical Cylinder Number, High Byte
LCNL	Logical Cylinder Number, Low Byte
LHN	Logical Head Number
LSN	Logical Sector Number
IST	Interrupt Status Byte
MODE	Mode
DTLH	Data Length, High Byte
DTLL	Data Length, Low Byte
ETN	Ending Track Number
ESN	Ending Sector Number
GPL2	Gap Length Two
RWCL	Write Current Cylinder, Low Byte
RWCH	Write Current Cylinder, High Byte
UST	Unit Status Byte
MGPL1	Modified Gap Length 1

3.1.3.5 LAYOUT RESULT AREA HD

COMMAND-	READ WRITE	READ ID	RECAL	SEEK	FORMAT	SPECIFY	SENSE INT. STAT	DETECT ERROR	SENSE UNIT STAT
RESD	7 CB- 6 0= 5 0 4 SRQ- 3 RRQ- 2 IER- 1 NCI- 0 DRQ-	-STR	-STR	-STR	-STR	-STR	-STR	-STR	-STR
RESD+1	7 ENC- 6 OVR- 5 DER- 4 EQC- 3 NR- 2 ND- 1 NWR- 0 MAM-	-EST			-EST		7 SKE 6 RC 5 SER 4 EQC 3 NR 2 UA2 1 UA1 0 UA0	EADH	7 6 5 4 DS 3 SC 2 TO 1 ROY 0 WFT
RESD+2	PHN	SCNT			SCNT			EADL	
+3	LCNH							EPAT1	
+4	LCNL							EPAT2	
+5	LHN							EPAT3	
+6	LSN								
+7	SCHT								

- STR STATUS REGISTER

CB = Command Busy
SRQ = Sense Interrupt Request
RRQ = Reset Request
IER = CRC error over ID
NCI = n.a.
DRQ = Data Request

INTERRUPT STATUS

SKE = Seek End
RC = Ready Change
SER = Seek Error
EQC = Drive fault
NR = Not Ready
UA 0, 1, 2 = Unit address

- EST ERROR STATUS

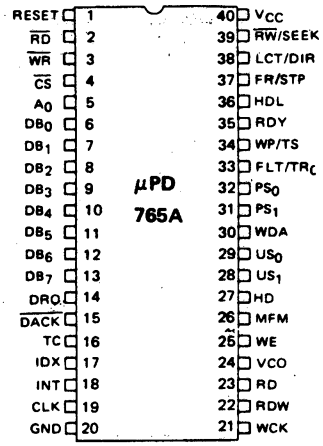
ENC = End of Cycle
OVR = Overrun
DER = ECC error
EQC = Drive Fault
NR = Not Ready
ND = Sector not found
NWR = Not writable
MAM = Data address mark not found

UNIT STATUS

DS = Drive Selected
SC = Seek Complete
To = Track o
RDY = Ready
WFT = Write Fault

3.1.4 FDC (FLOPPY DISK CONTROLLER 765)

3.1.4.1 PIN CONFIGURATION



μPD765A

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	INPUT/ OUTPUT	CONNECTION TO	FUNCTION
1	RST	Reset	Input	Processor	Places FDC in idle state. Resets output lines to FDD to "0" (low). Does not effect SRT, HUT or HLT in Specify command. If RDY pin is held high during Reset, FDC will generate interrupt 1-25 ms later. To clear this interrupt use Sense Interrupt Status command.
2	$\overline{RD}$	Read	Input (1)	Processor	Control signal for transfer of data from FDC to Data Bus, when "0" (low).
3	$\overline{WR}$	Write	Input (1)	Processor	Control signal for transfer of data to FDC via Data Bus, when "0" (low).
4	$\overline{CS}$	Chip Select	Input	Processor	IC selected when "0" (low), allowing $\overline{RD}$ and $\overline{WR}$ to be enabled.
5	A_0	Data/Status Reg Select	Input (1)	Processor	Selects Data Reg (A_0=1) or Status Reg (A_0=0) contents of the FDC to be sent to Data Bus.
6-13	DB_0-DB_7	Data Bus	Input/ (1) Output	Processor	Bi-Directional 8-Bit Data Bus.
14	DRQ	Data DMA Request	Output	DMA	DMA Request is being made by FDC when DRQ="1".
15	$\overline{DACK}$	DMA Acknowledge	Input	DMA	DMA cycle is active when "0" (low) and Controller is performing DMA transfer.
16	TC	Terminal Count	Input	DMA	Indicates the termination of a DMA transfer when "1" (high). It terminates data transfer during Read/Write/Scan command in DMA or interrupt mode.
17	IDX	Index	Input	FDD	Indicates the beginning of a disk track.
18	INT	Interrupt	Output	Processor	Interrupt Request Generated by FDC.
19	CLK	Clock	Input		Single Phase 8 MHz Squarewave Clock.
20	GND	Ground			D.C. Power Return.
21	WCK	Write Clock	Input		Write data rate to FDD. FM = 500 kHz, MFM = 1 MHz, with a pulse width of 250 ns for both FM and MFM.
22	RDW	Read Data Window	Input	Phase Lock Loop	Generated by PLL, and used to sample data from FDD.
23	RDD	Read Data	Input	FDD	Read data from FDD, containing clock and data bits.
24	VCO	VCO Sync	Output	Phase Lock Loop	Inhibits VCO in PLL when "0" (low), enables VCO when "1."
25	WE	Write Enable	Output	FDD	Enables write data into FDD.
26	MFM	MFM Mode	Output	Phase Lock Loop	MFM mode when "1," FM mode when "0."
27	HD	Head Select	Output	FDD	Head 1 selected when "1" (high), Head 0 selected when "0" (low).
28,29	US_1,US_0	Unit Select	Output	FDD	FDD Unit Selected.
30	WDA	Write Data	Output	FDD	Serial clock and data bits to FDD.
31,32	PS_1,PS_0	Precompensation (pre-shift)	Output	FDD	Write precompensation status during MFM mode. Determines early, late, and normal times.
33	FLT/TR_0	Fault/Track 0	Input	FDD	Senses FDD fault condition, in Read/ Write mode; and Track 0 condition in Seek mode.
34	WP/TS	Write Protect/ Two-Side	Input	FDD	Senses Write Protect status in Read/Write mode; and Two Side Media in Seek mode.
35	RDY	Ready	Input	FDD	Indicates FDD is ready to send or receive data.
36	HDL	Head Load	Output	FDD	Command which causes read/write head in FDD to contact diskette.
37	FR/STP	Fit Reset/Step	Output	FDD	Resets fault F.F. in FDD in Read/Write mode, contains step pulses to move head to another cylinder in Seek mode.
38	LCT/DIR	Low Current/ Direction	Output	FDD	Lowers Write current on inner tracks in Read/Write mode, determines direction head will step in Seek mode. A fault reset pulse is issued at the beginning of each Read or Write command prior to the occurrence of the Head Load signal.
39	$\overline{RW}$/SEEK	Read Write/SEEK	Output	FDD	When "1" (high) Seek mode selected and when "0" (low) Read/Write mode selected.
40	V_{CC}	+5V			DC Power.

Note: (1) Disabled when CS = 1.

3.1.4.2 FDC-COMMANDS USED

From the 15 available commands the ones listed below are used by the control unit

Used FDC-commands

1. Read data
2. Write data
3. Write Delete Data
4. Read ID
5. Write ID (Format Write)
6. Seek
7. Recallibrate
8. Sense Interrupt Status*
9. Specify
10. Sense Device Status

* May only be given as FDC interrupt is pending else it is interpreted as an invalid command.

3.1.4.3 LAYOUT FD-COMMAND AREA (MICRO-PROGRAM)

COMMAND-	READ	WRITE	READ DL.DAT	WRITE DL.DAT	READ ID	FORMAT	SEEK	RECAL	SENSE INT	SENSE DEV	SPECIFY
COMD	7 MT 6 MF 5 SK 4 0	7 0 6 MF 5 0 4 0	7 MT 6 MF 5 SK 4 0	MT MF 0 0	0 MF 0 0	0 MF 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
	3 0 2 1 1 1 0 0	1 3 1 2 0 1 1 0	1 1 0 0	1 0 0 1	1 0 1 0	1 1 0 1	1 1 1 1	0 1 1 1	1 0 0 0	0 1 0 0	0 0 1 1
COMD+1	7 0 6 0 5 0 4 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0		0 0 0 0	SRT
	3 0 2 HD 1 US1 0 US0	0 HD US1 US0	0 HD US1 US0	0 HD US1 US0	0 HD US1 US0	0 HD US1 US0	0 HD US1 US0	0 0 US1 US0		0 HD US1 US0	HUT
COMD+2	C	C	C	C		N	NCN				HLT-ND (7) (1)
COMD+3	H	H	H	H		SC					
COMD+4	R	R	R	R		GPL					
COMD+5	N	N	N	N		D					
COMD+6	EOT	EOT	EOT	EOT							
COMD+7	GPL	GPL	GPL	GPL							
COMD+8	DTL	DTL	DTL	DTL							

MT = Multirack
MF = MFM mode
SK = Skip DDAM (Deleted Data Mark)
HD = Head number
US 0, 1 = Drive number
C = Cylinder number
H = Head number
R = Sector number
N = Data length in one sector
EOT = End of Track
GPL = Gap Length
DTL = Data per sector to be processed

SC = number of sectors per track
D = Data pattern to be written in data area
NCN = New Cylinder Number
SRT = Step Rate Time
HUT = Head Unload Time
HLT = Head Load Time
ND = DMA mode

3.1.4.4 RESULT AREA FD

COMMAND	READ/READID/WRITE/WR.DEL.D		FORMAT	SPECIFY SEEK RECAL	SENSE INT.	SENSE DEV. STATUS	
RESD	7	0 =				7	FT=
	6	0				6	WP=
	5	SE =				5	RY=
	4	EC =	--STO		--STO	4	TO=
	3	NR =				3	TS=
	2	HD =				2	HD=
	1	UNIT				1	UNIT
	0					0	)
RESD+1	7	EN =			PCN		
	6	X					
	5	DE =	--ST1				
	4	OR =					
	3	X					
	2	ND =					
	1	NW =					
	0	MA =					
RESD+2	7	X					
	6	CM =					
	5	DD =	--ST2				
	4	NC =					
	3	SH =					
	2	SN =					
	1	BC =					
	0	MD =					
RESD+3	C		X				
RESD+4	H		X				
RESD+5	R		X				
RESD+6	N		N				
RESD+7							

STO : STATUS REGISTER 0
ST1 : STATUS REGISTER 1
ST2 : STATUS REGISTER 2
ST3 : STATUS REGISTER 3

3.1.4.5 STATUS REGISTERS

STATUS REGISTER 0

D7	Interrupt Code	IC	D7 = 0 and D6 = 0 Normal Termination of Command (NT) Command was completed and properly executed.
D6			D7 = 0 and D6 = 1 Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed.
			D7 = 1 and D6 = 0 Invalid command issue, (IC). Command which was issued was never started.
			D7 = 1 and D6 =1 Abnormal Termination because during command execution the ready signal from FDD changed state.
D5	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to 1 (high).
D4	Equipment Check	EC	If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recallibrate Command) then this flag is set.
D3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D1	Unit Select 1	US 1	These flags are used to indicate a Drive Unit.
D0	Unit Select 0	US 0	Number at Interrupt.

STATUS REGISTER 1

D7	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D6			Not used. This bit is always 0 (low).
D5	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D4	Over Run	OR	If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set.
D3			Not used. This bit always 0 (low).
D2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set.
			During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set.
			During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.
D1	Not Writable	NW	During execution of WRITE DATA, WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set.
			If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.

STATUS REGISTER 2

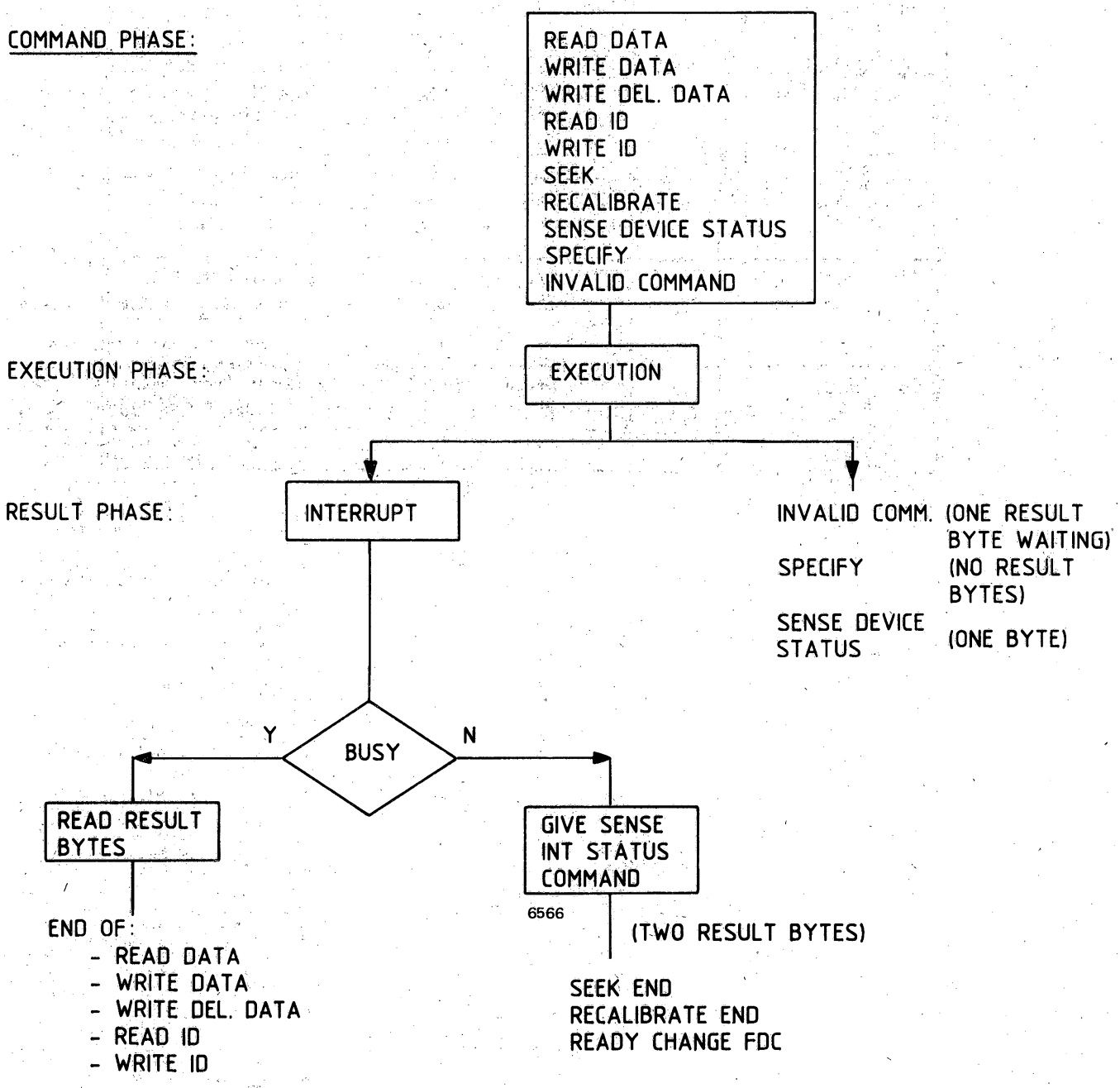
D7			Not used. This bit is always 0 (low).
D6	Control Mark	CM	During executing the READ DATA or SCAN Command, if the FDC encounters a Sector which contains a Deleted Data Address Mark, this flag is set.
D5	Data Error Data Field	DD	If the FDC detets a CRC error in the data field then this flag is set.
D4	Wrong Cynlinder	WC	This bit is related with the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
D3	Scan Equal Hit	SH	During execution, the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
D2	Scan Not Satisfied	SN	During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
D1	Bad Cylinder	BC	This bit is related with the ND bit, and when the contents of C on the medium is different from that stored in the IDR and the contents of C is FF, then this flag is set.
D0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.

STATUS REGISTER 3

D7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D5	Ready	RY	This bit is used to indicate the status of the Ready signal from the FDD.
D4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD
D3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D2	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D1	Unit Select 1	US 1	This bit is used to indicate the status of the Unit select 1 signal to the FDD.
D0	Unit Select 0	US 0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

3.1.4.6 GENERAL FLOW FO FD-COMMAND

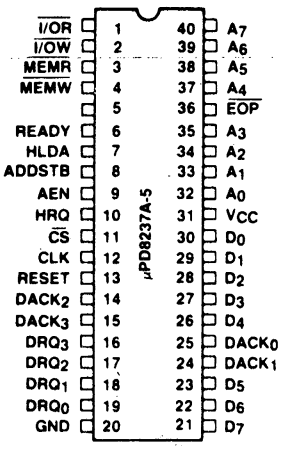
As indicated in the tables given before, the data necessary for a certain command is stored in the command area COMD till COMD+8.
The variable STAT8 gives the number of bytes which has to be sent to the FDC for a certain command.
After the command phase the FDC likes to report the result of the command executed.
Most of the commands leave the execution phase b.m.o. an interrupt, some not.



3.1.5 DMA (DIRECT MEMORY ACCESS CONTROLLER 8237)

3.1.5.1 PIN CONFIGURATION

Pin Configuration



Pin Identification

No.	Symbol	Direction	Function
1	$\overline{I/OR}$	IN/OUT	In Idle state, $\overline{I/OR}$ is an input control line used by the CPU to read control registers. In Active state, the μPD8237A-5 uses $\overline{I/OR}$ as an output control signal to access data from a peripheral during a DMA Write.
2	$\overline{I/OW}$	IN/OUT	In Idle state, the CPU uses $\overline{I/OW}$ as an input control signal to load information to the μPD8237A-5. In Active state, the μPD8237A-5 uses $\overline{I/OW}$ as an output control signal to load data to a peripheral during a DMA Read. The rising edge of $\overline{WR}$ must follow each data byte transfer in order for the CPU to write to the μPD8237A-5. Holding $\overline{I/OW}$ low while toggling $\overline{CS}$ does not produce the same effect.
3	$\overline{MEMR}$	OUT	$\overline{MEMR}$ accesses data from a specified memory location during memory-to-peripheral or memory-to-memory transfers.
4	$\overline{MEMW}$	OUT	$\overline{MEMW}$ writes data to a specified memory location during peripheral-to-memory or memory-to-memory transfers.
5		IN	Pin 5 is always tied high.
6	READY	IN	The READY signal can extend memory read and write pulses for slow memories or I/O peripherals.
7	HLDA	IN	HLDA indicates that the CPU has relinquished control of the system buses.
8	ADDSTB	OUT	This signal strobes the upper address byte from D_0-D_7 into an external latch.
9	AEN	OUT	This signal allows the external latch to output the upper address byte by disabling the system bus during DMA cycles. You should use HLDA and AEN to deselect I/O peripherals that may be erroneously accessed during DMA transfers. The μPD8237A-5 deselects itself during DMA transfers.
10	HRQ	OUT	This signal requests control of the system bus. The μPD8237A-5 issues this signal in response to software requests or DRQ inputs from peripherals.
11	$\overline{CS}$	IN	The CPU uses $\overline{CS}$ to select the μPD8237A-5 as an I/O device during an I/O Read or Write by the CPU. This provides CPU communication on the data bus. $\overline{CS}$ may be held low during multiple transfers to or from the μPD8237A-5 as long as $\overline{I/OR}$ or $\overline{I/OW}$ is toggled following each transfer.
12	CLK	IN	Controls internal operations and data transfer rate.
13	RESET	IN	Clears the Command, Status, Request, and Temporary registers, the first/last flip/flop, and sets the Mask register. The μPD8237A-5 is in Idle state after a Reset.
14, 15 24, 25	$DACK_0$- $DACK_3$	OUT	These lines indicate an active channel. They are sometimes used to select a peripheral. Only one DACK may be active at any time. All DACK lines are inactive unless DMA has control of the bus. You may program the polarity of these lines; however, Reset initializes them to active low.
16-19	DRQ_0-DRQ_3	IN	These are asynchronous channel request inputs used by peripherals to request DMA service. In a Fixed Priority scheme, DRQ_0 has the highest priority and DRQ_3 has the lowest. You may program the polarity of these lines; however, Reset initializes them to active high.
20	GND		Ground.
21-23, 26-30	D_0-D_7	IN/OUT	During an I/O Read, the CPU enables these lines as outputs, allowing it to read an Address register, a Word Count register, or the Status or Temporary register. During an I/O Write, these lines are enabled as inputs, allowing the CPU to program the μPD8237A-5 control registers. During DMA cycles, the eight MSBs of the address are output to the data bus to be strobed to an external latch via ADDSTB.
31	V_{CC}		Power Supply.

3.1.5.2. DMA GENERAL

The DMA has 4 channels CH0---3

Use of channels:

CH0/1, Mem to Mem, MM to LM (see note)
                   or LM to MM

  CH2, HDC write, LM to HDC
        HDC Read, HDC to LM
  CH3, FDC write, LM to FDC
        FDC read, FDC to LM

Note: MM = Main Memory
      LM = Local Memory

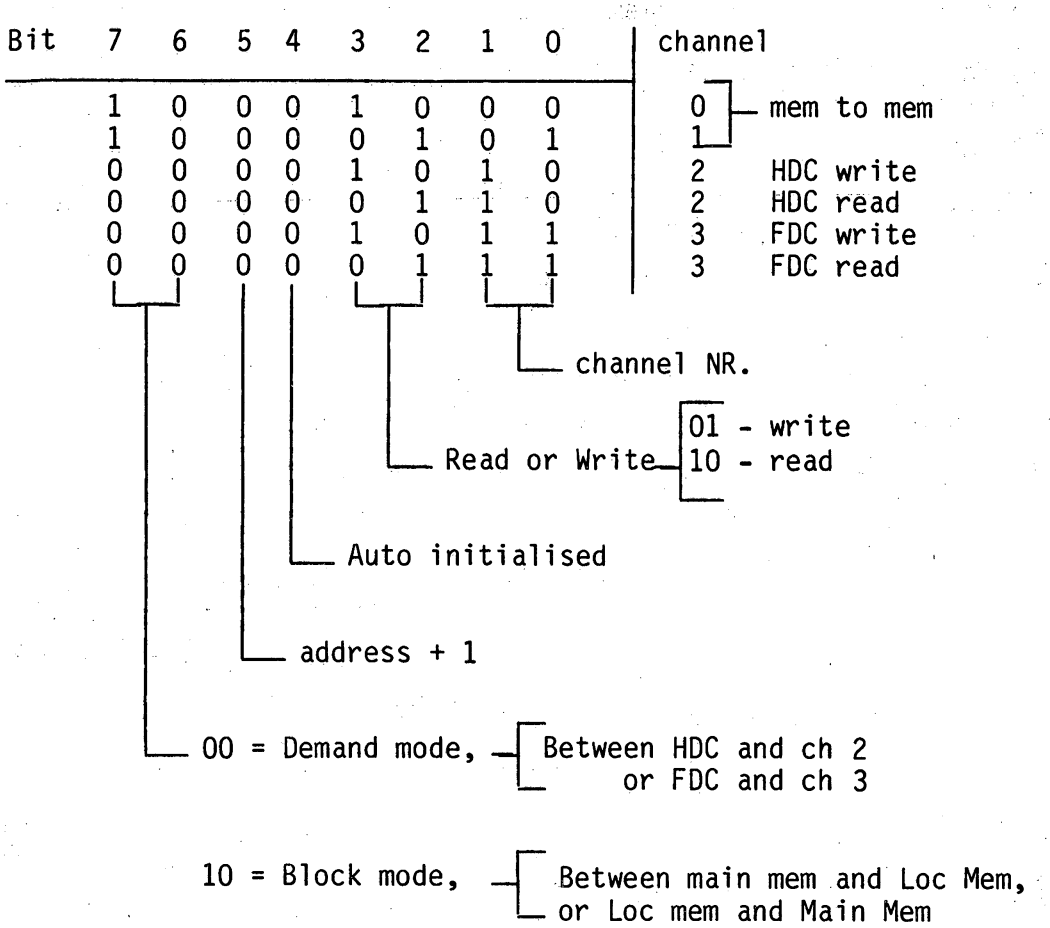
To program the DMA channels, the following registers are used.
MNEM is the mnemonic used by the micro program.

3.1.5.3 WRITE "COMMAND" REG. (MNEM : DMACR)

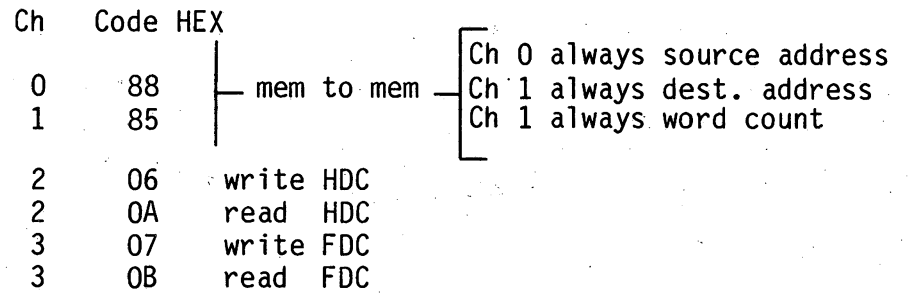
Used codes:

00H   non mem to mem
01H   mem to mem
04H suppress DMA action ch 0
05H suppress DMA action ch 1

Used codes:



Resume: Mode Reg.



3.1.5.5 WRITE "REQUEST" REGISTER (MNEM : DMARR)

Used code:

04 H for software request Ch 0, i.c.o. mem to mem

3.1.5.6 WRITE "MASK" REGISTER

1) Write "Single mask bit" (MNEM : DMAAR)
   to enable/disable DRQ, for 1 channel.

Used code:

Ch	Enable DRQ	Disable DRQ
0	00	04
1	01	05
2	02	06
3	03	07

2) Write "All Mask bits" (MNEM : DMAAM)

To enable/disable DRQ, for all channels

Used code: (bit configuration)

```
0 0 0 0    X X X X      X = 1 = Disable DRQ
Channel    3 2 1 0      X = 0 = Enable  DRQ
```

3.1.5.7 ADDRESS AND WORD COUNT

Each channel has an address and word count register.

Write base and current address (MNEM : DMABO...3)
Write base and current word count (MNEM : DMACO...3)

Note: For Mem to Mem, two channels are used, CH 0 and CH 1.

In both cases, MM to LM and LM to MM,
CH 0 is the source.
CH 1 is the destination and word count

3.2 HARDWARE

3.2.1 GENERAL

In this description often will be referred to the functional diagams of this control unit. See chapter 4.

The main parts are described in:

3.2.2 CONTROL PART

3.2.3 HARD DISK CONTROL

3.2.4 FLOPPY DISK CONTROL

3.2.5 DATA HANDLING FROM DISK

3.2.6 UPL-PART

3.2.2 CONTROL PART

3.2.2.1 LOADING/READ OUT FDC, HDC, DMA AND REGISTERS

The figure below indicates which IO-addresses are used for the parts connected.

IO-addresses -----		7	6	5	4	3	2	1	0
DMA-unit (8237A)	00: 0F	-	-	-	-	X	X	X	X
FDC (765A)	40, 41	-	1	-	-	-	-	-	X
HDC (7261)	80, 81	1	-	-	-	-	-	-	X
Miscellaneous	C0: CF	1	1	-	-	X	X	X	X

The next table gives the function of all IO-address used.

3.2.2.2 TABLE OF ALL I/O ADDRESSES USED

DMA 00:0F	IO - address	IORN	IOWN	Function	Mnemonic
CH0	00	1	0	Write base and current address	DMABO
	00	0	1	Read current address	DMABO
	01	1	0	Write base and current word count	DMACO
	01	0	1	Read current word count	DMACO
CH1	02	1	0		DMA B1
	02	0	1	Same for channel 1	DMA B1
	03	1	0		DMA C1
	03	0	1		DMA C1
CH2	04	1	0		DMA B2
	04	0	1	Same for channel 2	DMA B2
	05	1	0		DMA C2
	05	0	1		DMA C2
CH3	06	1	0		DMA B3
	06	0	1	Same for channel 3	DMA B3
	07	1	0		DMA C3
	07	0	1		DMA C3
	08	0	1	Read Status Register	DMA SR
	08	1	0	Write Command Register	DMA CR
	09	1	0	Write Request Register	DMA RR
	0A	1	0	Write Single Mask bit	DMA AR
	0B	1	0	Write Mode Register	DMA MR
	0C	1	0	Clear Byte Pointer FF	DMA BP
	0D	0	1	Read Temp. Register	DMA TR
	0E	1	0	Master Clear	DMA MC
	0F	1	0	Write all Mask bits	DMA AM
FDC 40, 41					
	40	0	1	Read Status Register	FD RSR
	41	0	1	Read Data Register	FD RDR
	41	1	0	Write Data Register	FD WDR
HDC 80, 81					
	80	0	1	Read Data fifo	HD RDF
	80	1	0	Write Data fifo	HD WDF
	81	0	1	Read Status Register	HD RSR
	81	1	0	Write command Register	HD WCR

3.2.2.3 ADDRESSABLE LATCH LS259

IO - address	IORN	IOWN	Function	Mnemonic
C0	1	0	Set MODE0	MODE0
C1	1	0	Set WRINT, W/R UPL	WRINT
C2	1	0	Set HDFD, Hard disk/Floppy disk	HDFD
C3	1	0	Set MOTONB, FD motor	MOTON
C4	1	0	ENDTIRN	EDTI
C5	1	0	WNDTIRN	WDTIR
C6	1	0	Set DOORLO, doorlock drive 0	DOOR0
C7	1	0	Set HS03, head Select 3 HD	DOOR1

MODE0 : 0 = DMA actions between FDC/HDC and Local Memory.
1 = DMA actions between Local Memory and UPL-bus (MM).

WRINT : 0 = UPL read operation.
1 = UPL write operation.

HDFD : 0 = Hard disk selected.
1 = Floppy disk selected.

MOTONB : 0 = Motor floppy drive off.
1 = Motor floppy drive on.

ENDTIRN : 0 = Enable DTI Ram
1 = Disable DTI Ram
WDTI RN : 0 = Enable Write DTI Ram
1 = Disable Write DTI Ram

DOORLO : 0 = Unlock drive 0.
1 = Lock drive 0.

HS03 : 0 = HS3 becomes '1'.
1 = HS3 becomes '0'.

3.2.2.4 DECODER LS138

IO - Address	IORN	IOWN	Function	Mnemonic
C8	1	0	Set SCHAN, Set charc. mode	CHAN
C9	1	0	Give STIHCN, Start IHC inter. for Int. Destination Addr. bit 5 = 0	IHCD
E9	1	0	Give STIHCN, Start IHC inter. for Int. Source Addr. bit 5 = 1	IHCS
CA	1	0	Give RESTFN, Reset Start FF, BUS LSI	RESTF
CB	1	0	Give LMADEN. Load MADE register	MADE
CC	1	0	Give UPEOPN, EOP	EOP
CD	1	0	Give RWTFN, Reset fault FF	RWTF
CE	1	0	RDCH0, Reset disk change FD0	RDCH0
CF	1	0	RDCH1, Reset disk change FD1	RDCH1

3.2.2.5 C.U STATUS LS244

IO - address	IORN	IOWN	Function	Mnemonic
C0	0	1	Read CU Status UIORN	RSCU

```
================================================
INPUT 0 = STARTF      START FF
      1 = INTFN       Interrupt FF
      2 = WFLT        Write Fault FF
      3 = CONNECT     DTI connected
      4 = DICH0       Disk Change from floppy 0
      5 = DICH1       Disk Change from floppy 0
      6 = HDFD        Hard Disk or Floppy Disk
      7 = HSNS        High/Normal Speed floppy
```

3.2.2.6 SELECTION DECODES, ADDRESSABLE LATCHES ETC.

The selection of the decoders and addressable latches is in hardware done as indicated in the figure below.

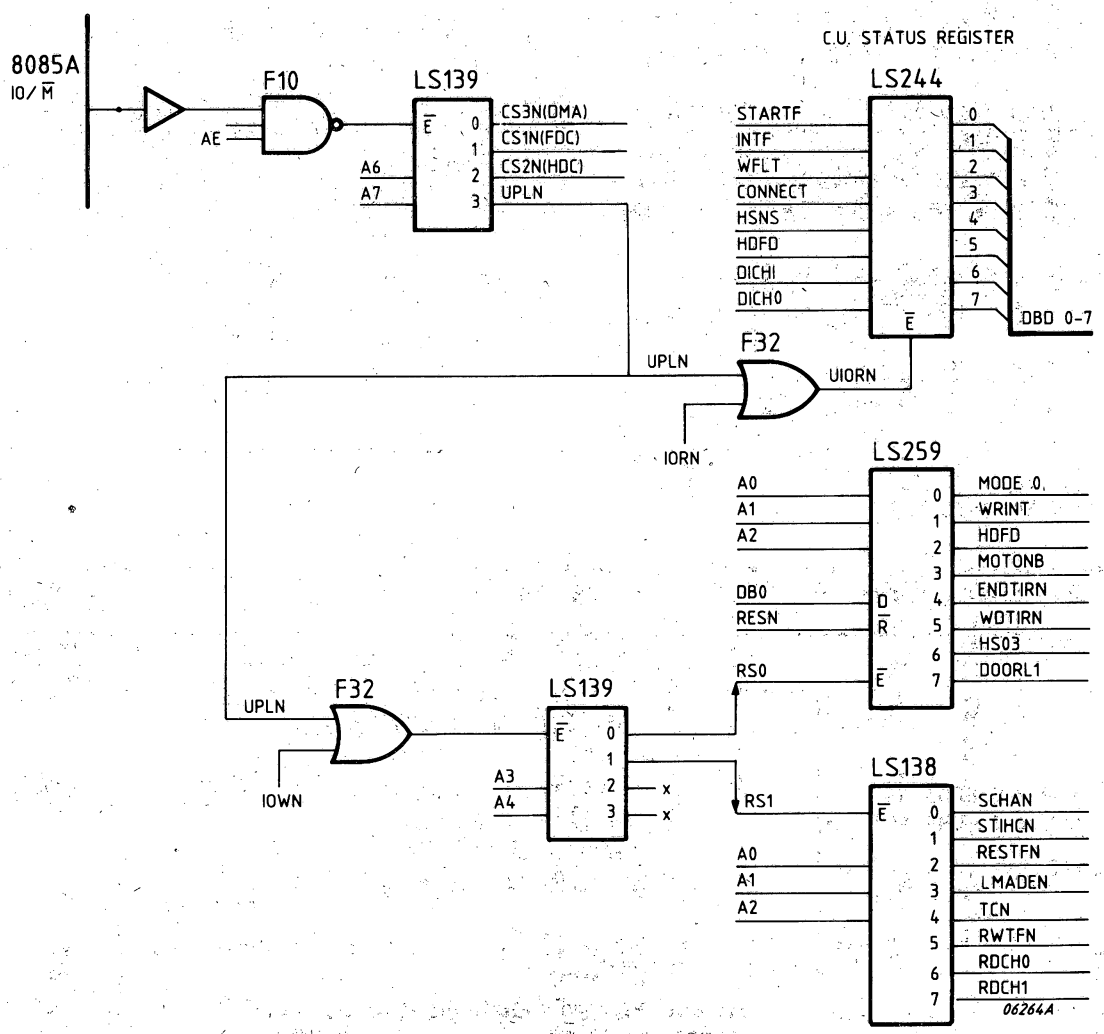


Figure 3.1 SELECTION DECODERS, ADDRESSABLE LATCHES ETC.

3.2.2.7 LOCAL RAM AND EPROM CONTROL

The EPROM 8K8 is mapped in the address range from 0 till 8K (0000H till 1FFFH); the local RAM (2K8) from 8K till 10K (2000H till 27FF).

The local RAM can be:

I. Read/written by the microprocessor.

II. Read/written by the DMA-unit during data to FDC/HDC.

III. Read/written by the DMA-unit during data transfer to the UPL-bus (MAIN MEMORY).

IV. Disabled as the DTI-AM has to be loaded (see DTI-part).

A part of the control is located in an FPLA (see contents FPLA1).

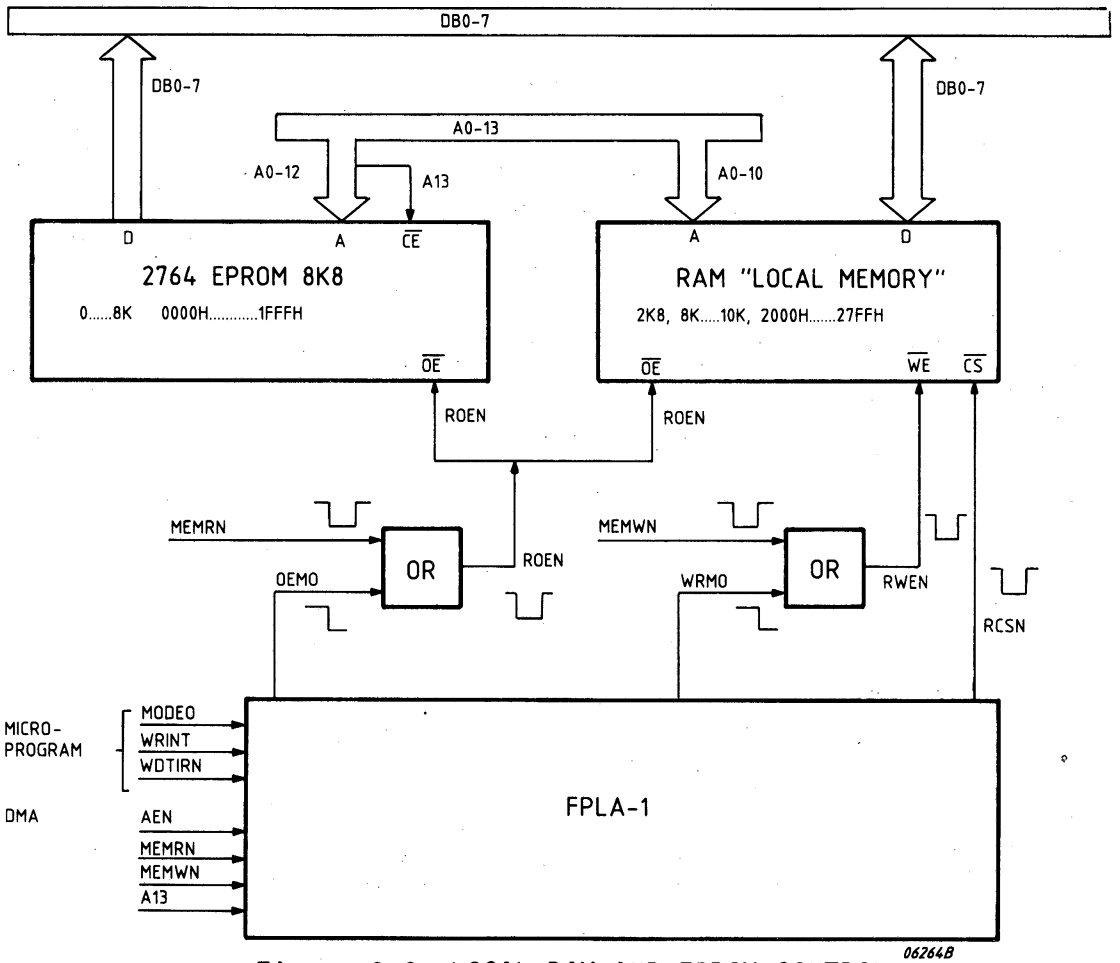


Figure 3.2 LOCAL RAM AND EPROM CONTROL

AEN = 0 8085 ACTIVE
AEN = 1 DMA ACTIVE

ENDIRN : 0 = Enable DTI Ram
1 = Disable DTI Ram

WDTIRN : 0 = Enable write DTI Ram
1 = Disable write DTI Ram

MODEO : 0 = DMA actions between FDC/HDC and Local Memory.
1 = DMA actions between Local Memory and UPL-bus (MM).

WRINT : 0 = UPL read operation.
1 = UPL write operation.

FPLA-1 LOC D2C9

INPUTS (PIN, NAME)										OUTPUT	
1	2	3	4	5	6	7	8	18	19		
WRINT	EOPN	AEN	MEMRN	MEMWN	MODEO	A13	AO	WDTIRN	TEST 1	PIN	NAME
										15	RCSN
X	X	X	⊓	1	X	1	X	1	1		⊓
X	X	X	1	⊓	X	1	X	1	1		⊓
										16	WRMO
1	X	1	X	X	1	X	X	X	1		1
										17	OEMO
0	X	1	X	X	1	X	X	X	1		1

X = Dont't Care
TEST 1 = 1 is an enable for FPLA-1 (STRAP for "GENRAD")

See fig 3.2 LOCAL RAM AND EPROM control
Note: WRMO = 1 Is a disable
OEMO = 1 Is a disable

3.2.2.8. DTI RAM CONTROL

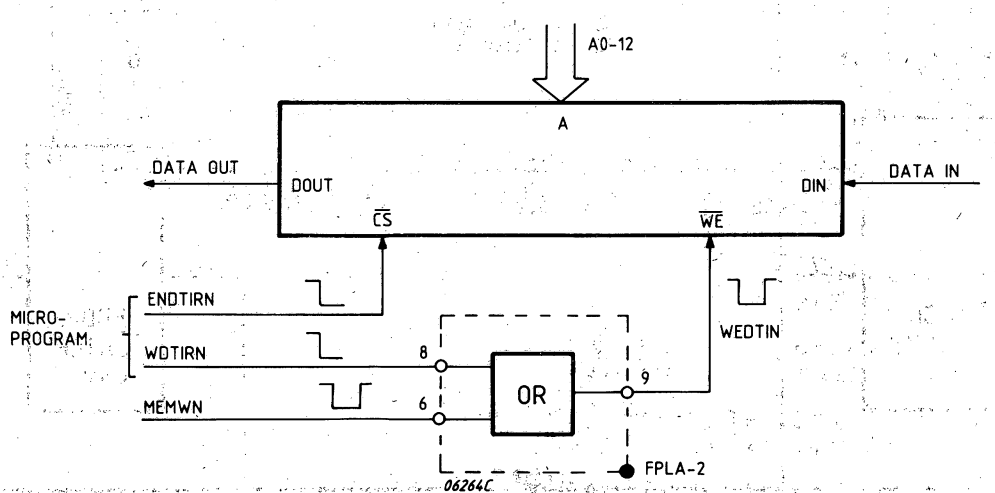


Figure 3.3 DTI RAM CONTROL

3.2.2.9 ADDRESS/DATA GENERATION AND IO/MEMORY CONTROL

As well the microprocessor (8085A) as the DMA-unit (8237A) can control the internal data/address bus and IO/Memory lines (see figure 3.4)

By means of HRQ line the DMA-unit request control, which is acknowledge by HLDA. Address A0:7 is generated directly by the DMA-unit; A8:15 by means of the data lines DBD0:7 which are latched by ADSTB.
AEN puts the IO/Memory lines and address buffer for address A0:7 in Hz-state, so they can be taken over by the DMA-unit.

For easy connection of DMA-unit and controllers the microprocessor operates in the non-memory mapped IO mode.
The IO/M line of the microprocessor determine if the memory lines MEMRN, MEMWN or the IORN, IOWN lines are active.

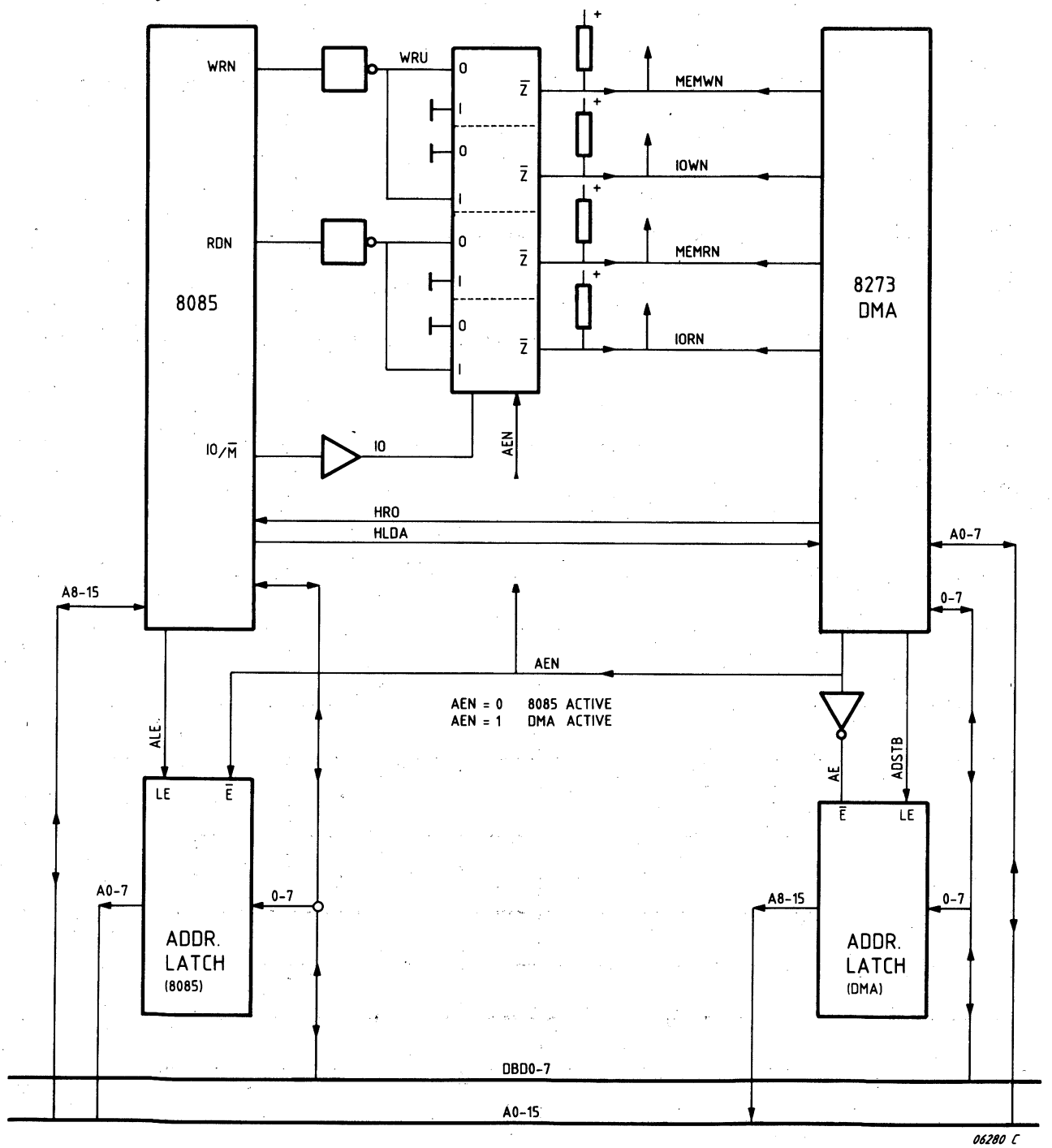


Figure 3.4 ADDRESS/DATA GENERATION AND IO/MEM CONTROL

3.2.2.10 FPLA-1 TABLE

FPLA-1 LOC D2C9

INPUTS (PIN, NAME)										OUTPUT
1	2	3	4	5	6	7	8	18	19	
WRINT	EOPN	AEN	MEMRN	MEMWN	MODEO	A13	AO	WDTIRN	TEST 1	PIN NAME
										9 CLSTRN
1	⊓	1	X	X	1	X	0	X	1	⊓
1	X	1	X	⊓	1	X	1	X	1	⊓
0	X	1	⊓	X	1	X	1	X	1	⊓
										11 LL07
1	X	1	X	X	1	X	0	X	1	0
										12 LL815
1	X	1	X	X	1	X	X	X	1	0
										13 E07
0	X	1	⊓	X	1	X	0	X	1	⊓
										14 E815
0	X	1	⊓	X	1	X	1	X	1	⊓
										15 RCSN
X	X	X	⊓	1	X	1	X	1	1	⊓
X	X	X	1	⊓	X	1	X	1	1	⊓
										16 WRMO
1	X	1	X	X	1	X	X	X	1	1
										17 OEMO
0	X	1	X	X	1	X	X	X	1	1

X = Don't care
TEST 1 = is an enable for FPLA-1 (STRAP for "GENRAD")

INPUTS PIN/NAME												OUTPUT
1	2	3	4	5	6	7	6	16	17	18	19	PIN NAME
TEST2	SDTU	CON-NECT	PFN	ODTIR	MEMWN	MEMRN	WDTIRN	REDY	REQB	MODE 0	WRINT	
												9 WEDT1N
1	X	X	X	X	⊓	X	0	X	X	X	X	⊓
												11 TRAP
1	X	X	⊓	X	X	X	X	X	X	X	X	⊓----
1	⊓	1	X	X	X	X	X	X	X	X	X	⊓----
1	X	1	X	0	⊓	X	1	X	X	X	X	⊓----
1	X	1	X	0	X	⊓	1	X	X	X	X	⊓----
1	X	X	X	X	X	X	⊓	X	X	X	X	---⊓
												12 MADLN
1	X	X	X	X	⊓	X	X	X	1	X	1	⊓
1	X	X	X	X	X	⊓	X	X	1	X	0	⊓
												13 MORQB
1	X	X	X	X	X	X	X	X	⊓	1	X	⊓
												14 WSTDMA
1	X	X	X	X	X	X	X	⊓	X	0	X	⊓

X = Don't care
TEST 2 = is an enable for FPLA-2 (STRAP for "GENRAD")

3.2.2.12 WAIT STATES 8085 AND DMA

- Wait state for 8085 during IO.

During an IO instruction to HDC or FDC, the 8085 has to wait a moment for data set up time inside the HDC or FDC.

This is done according to figure 3.5.

ALE = Address Latch Enable
CLGEN = Clock of 8085
If R8085 is low the 8085 waits.

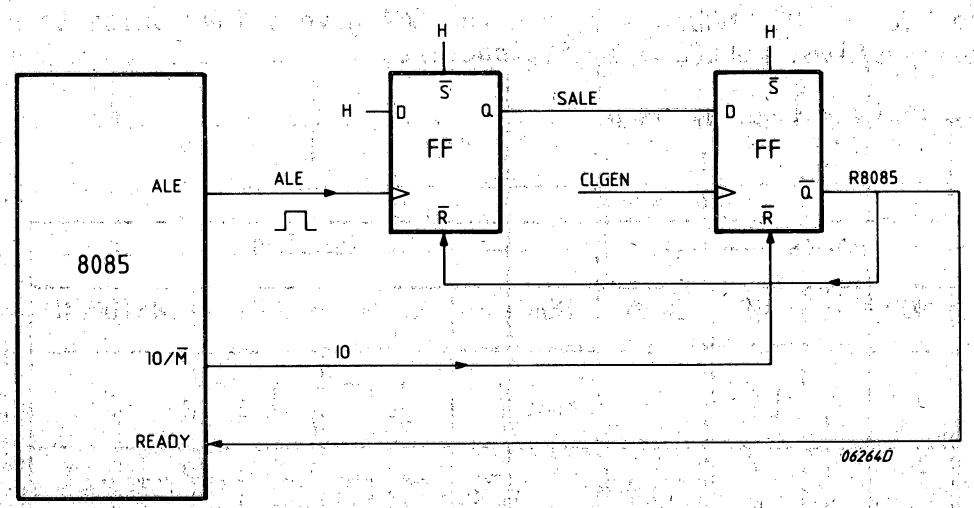


Figure 3.5 WAIT STATE FOR 8085 IN CASE OF IO

- Wait-state for DMA

a) DMA action, Main Mem. to Loc. Mem.
   Wait for transport from UPL-Bus into L.M.

b) DMA action, Write into HDC or FDC.
   Wait for transport from L.M. into HDC or FDC.

See next table and figure 3.6.

During MM to LM, MODEO = 1, and the BUS LSI give a REQB pulse to clock the data from UPL-BUS into the BIO input buffer.
IOWN is inactive.
Result: Redy to DMA is 1 clock of CL5 Low.

During LM to HDC or FDC, MODEO = 0, and the DMA give a IOWN pulse to reset RCLN.
REQB = 1, is inactive. MOREQB = 1, is inactive.

Result: Same. RCLN set by WSTDMAN.

	Inputs			Results			
	MODEO	REQB	IOWN	MOREQB	RCLN	REDY	WSTDMAN
a	1	⊓	1	⊓	⊓	⊓	1
b	0	1	⊓	1	⊓	⊓	⊓

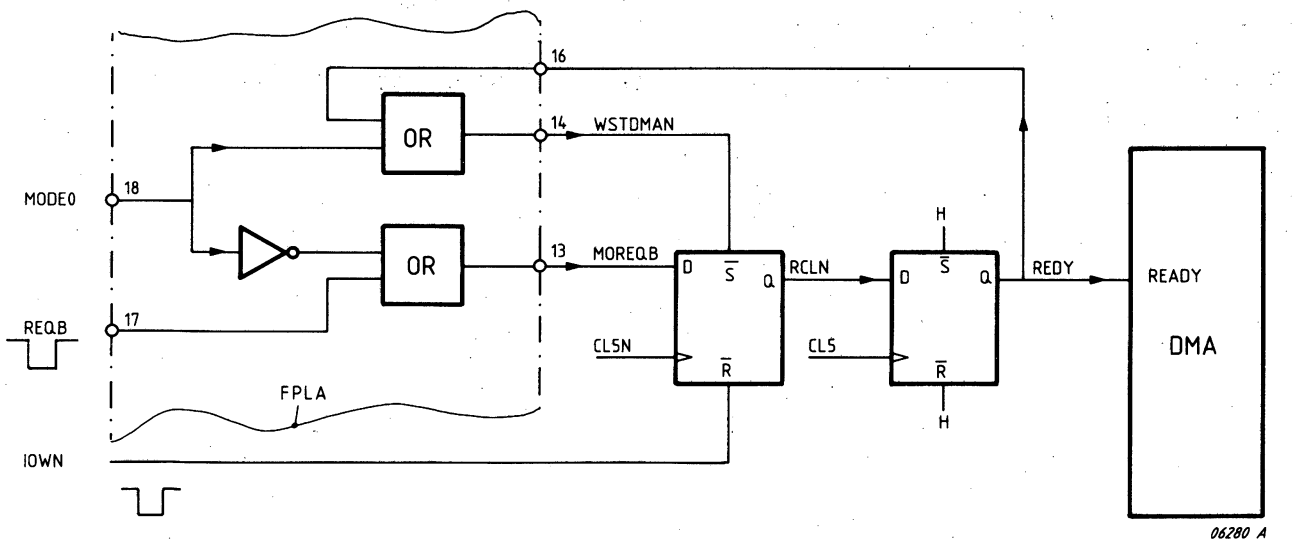


Figure 3.6 WAIT-STATE FOR DMA

3.2.2.13 WRITE FAULT DETECTION

As the control unit should edge detect the write fault signal a D-FF is added to do so (see figure below).

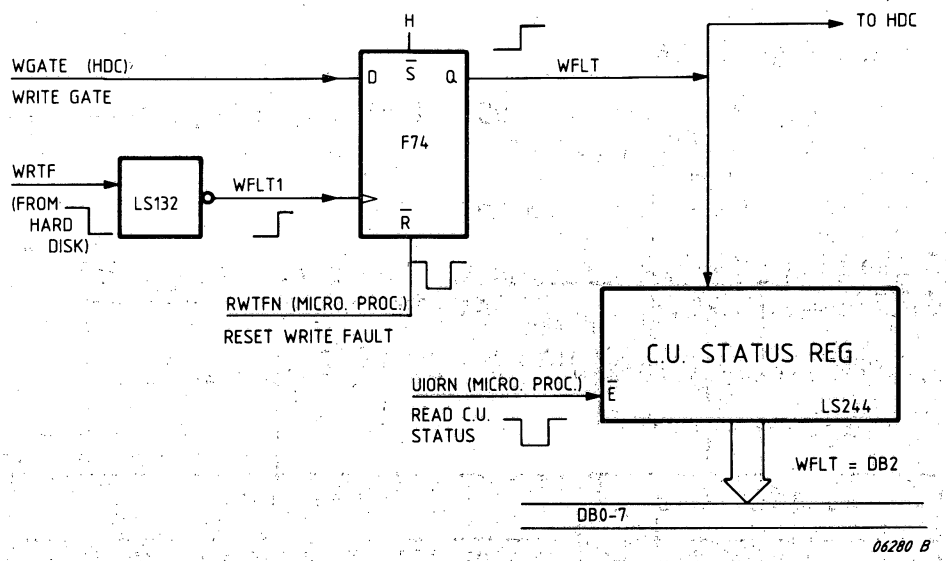


Figure 3.7 WRITE FAULT DETECTION

The falling edge of WRTF is latched by an F74 and sent to the HDC (WFLT).

WGATE = Write Enable for Disk

This condition is used as an protection for wrong detection of WFLT.

The microprocessor can read this FF, by generating mnemon. RSCU to the C.U. Status Reg, the hardware signal is UIORN.

The microprocessor can reset this FF again by generating mnem RWTF, the hardware signal is RWTFN.

3.2.2.14 UNIT HAS BEEN NOT READY DETECTION (HBNR)

For the floppy-disk drives a detection is added to see if there is a change in their state caused by e.g. opening the door and removing the diskette.
For this purpose the signal IUDCH has to be present on the floppy drive interface.
Below the hardware realization is given.

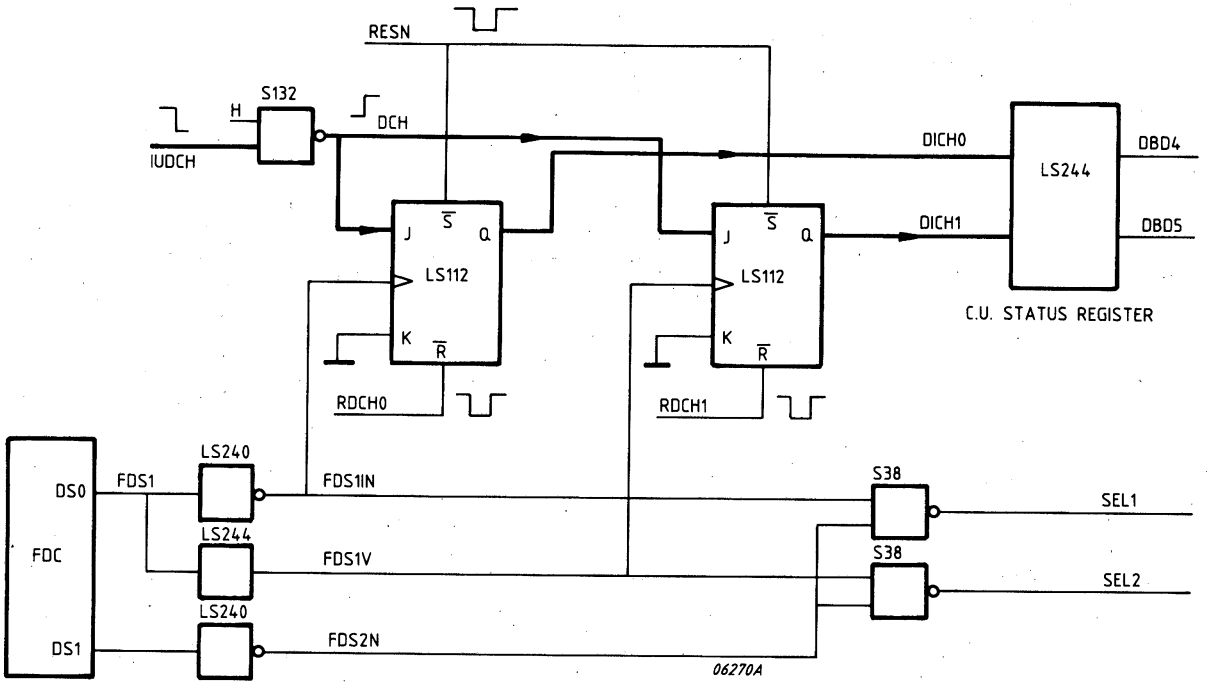


Figure 3.8 UNIT HAS BEEN NOT READY DETECTION

As one of the floppy drives is selected the signal IUDCH may go to a low level, indicating there is something wrong with the READY state and/or the door has been opened and/or the diskette has been removed. At the end of its selection the state of IUDCH is stored and stays there for investigation.

If a command is started, which results in a read or write to the drive and 'unit has been not ready' is detected the command is finished with a corresponding logical and physical status indication. Only by means of a 'TOPER' command for the concerning drive a reset is possible of the 'unit has been not ready' signal.

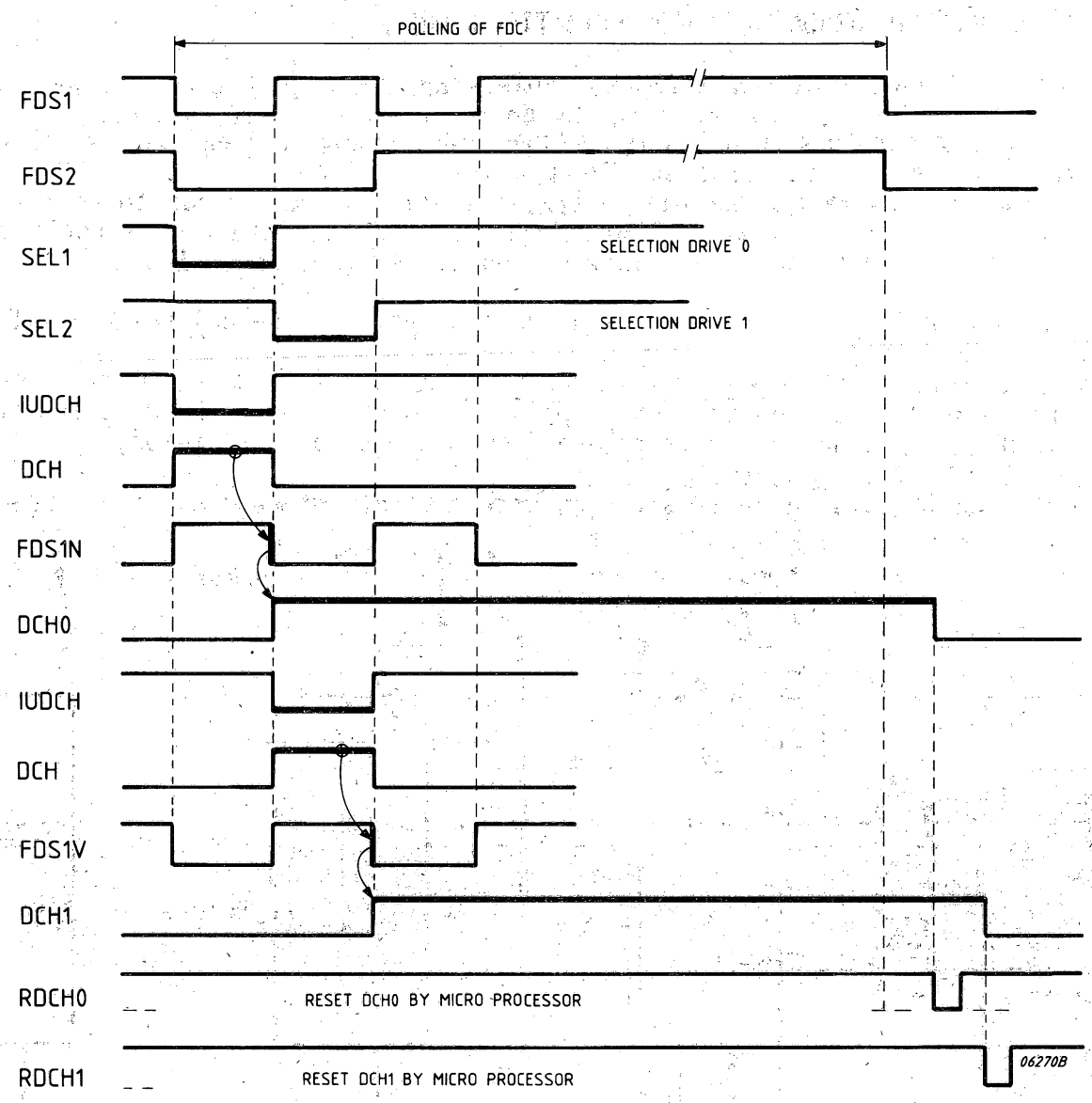


Figure 3.9 TIMING HBNR

After Power On or RSLN or CLEARN or RESETN (DT1) the DCHO and DCH1 are set 1.

Read out of DCHO and DCH1 is done b.m.o mnem RSCU (read C.U. Status) port CO HEX

Reset of DCHO and DCH1 is done by RDCHO and RDCH1 via the microprogram, port CE and CF HEX.

3.2.3 HARD DISK CONTROL

3.2.3.1 HDC RELATION TO 8085, DMA and LOCAL MEMORY

The hard disk control (HDC) chip (7261) can handle a hard sector disk (SMD interface) or a soft sector disk (Floppy-like interface).
In ower case we have to use the latest as the drives which has to be connected have a floppy like interface (ST506/412). Most of the interface signals can be directly connected (with proper drivers/receivers) (see sheet 140-2).

How the read/write data from/to the drive is handled is described in 3.2.5 (Data handling from disk).
This part describes how the microprocessor can activate the HDC to perform a certain command, also how the interrupt of the controller is handled and in what way the DMA-unit transport data to and from the HDC to local memory.

Below a simplified diagram is given of the parts of interest.

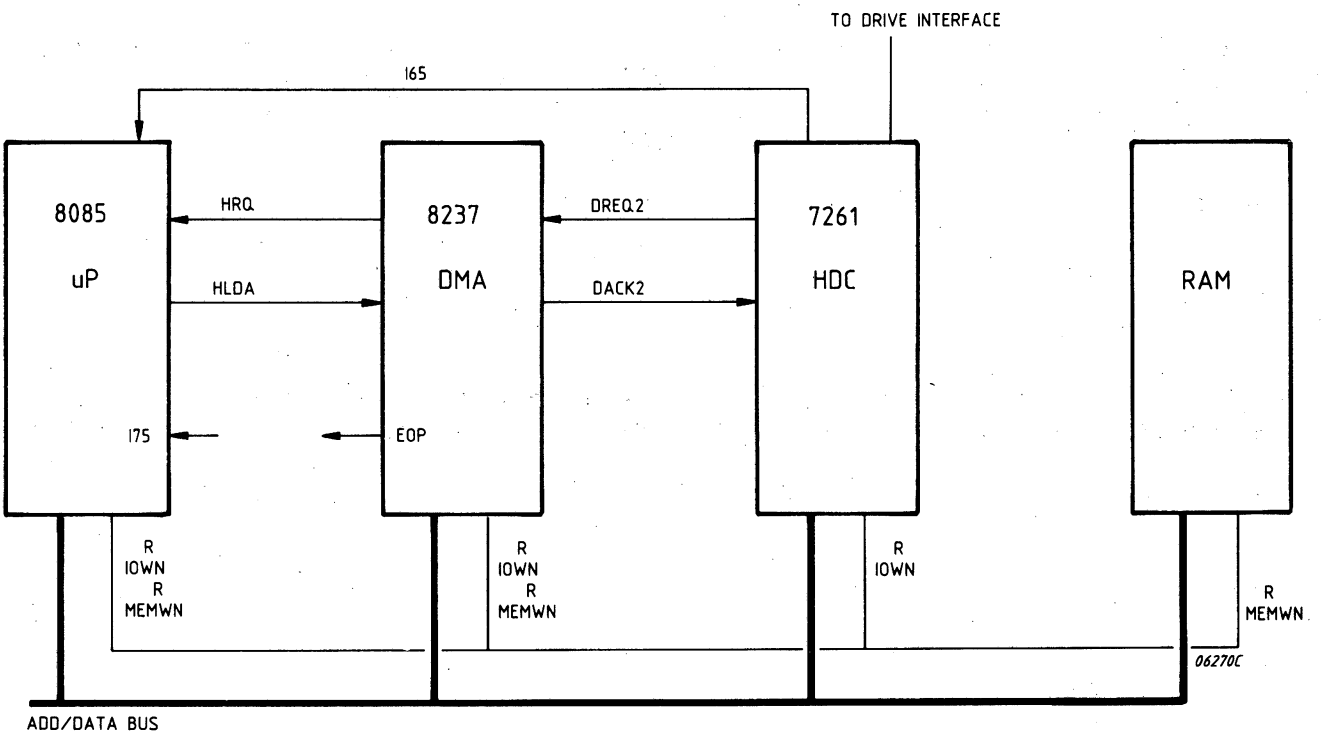


Figure 3.10 HDC RELATION TO 8085, DMA AND LOCAL MEM

As an example the main actions are described for a READ from disk.

A- We assume that the read action will be successfull so data has to be transported from the HDC to the local memory b.m.o. the internal data/address bus and the IOWN line. The main items we have to load are the local memory address from where the data has to be written and a word count to indicate how many bytes has to be transported.

B- Now a number of commmand bytes can be sent to the HDC to perform the read operation. This is done b.m.o. the address bus (Selects the right register), data bus and the IOWN line.

C- Now the microprocessor has to wait for the reaction of the DMA-unit and HDC. If everything goes without problems the HDC detects the sector of interest and will transport the data to local memory.
Therefore the HDC has to activate the DMA-unit b.m.o. DREQ2; the DMA has to perform the data transport and therefore a HRQ is sent to the microprocessor to take over the bus-control.

If all right the microprocessor answers with HLDA; now the DMA acknowledge, b.m.o. DACK2, to request of the HDC and the transport starts.
The DMA-unit generate IORN to the HDC and MEMWN to the local memory. This continuous till all data is transported.

Then the following happens:
- DMA generates EOP
- DREQ2 becomes non-active so control back to microprocessor.
- HDC gives interrupt I65 to microprocessor to inform about the result of the transport.

About the same happens with other commands which require DMA Transport of data. The microprogram gives of course more detailed information of these kind of actions.

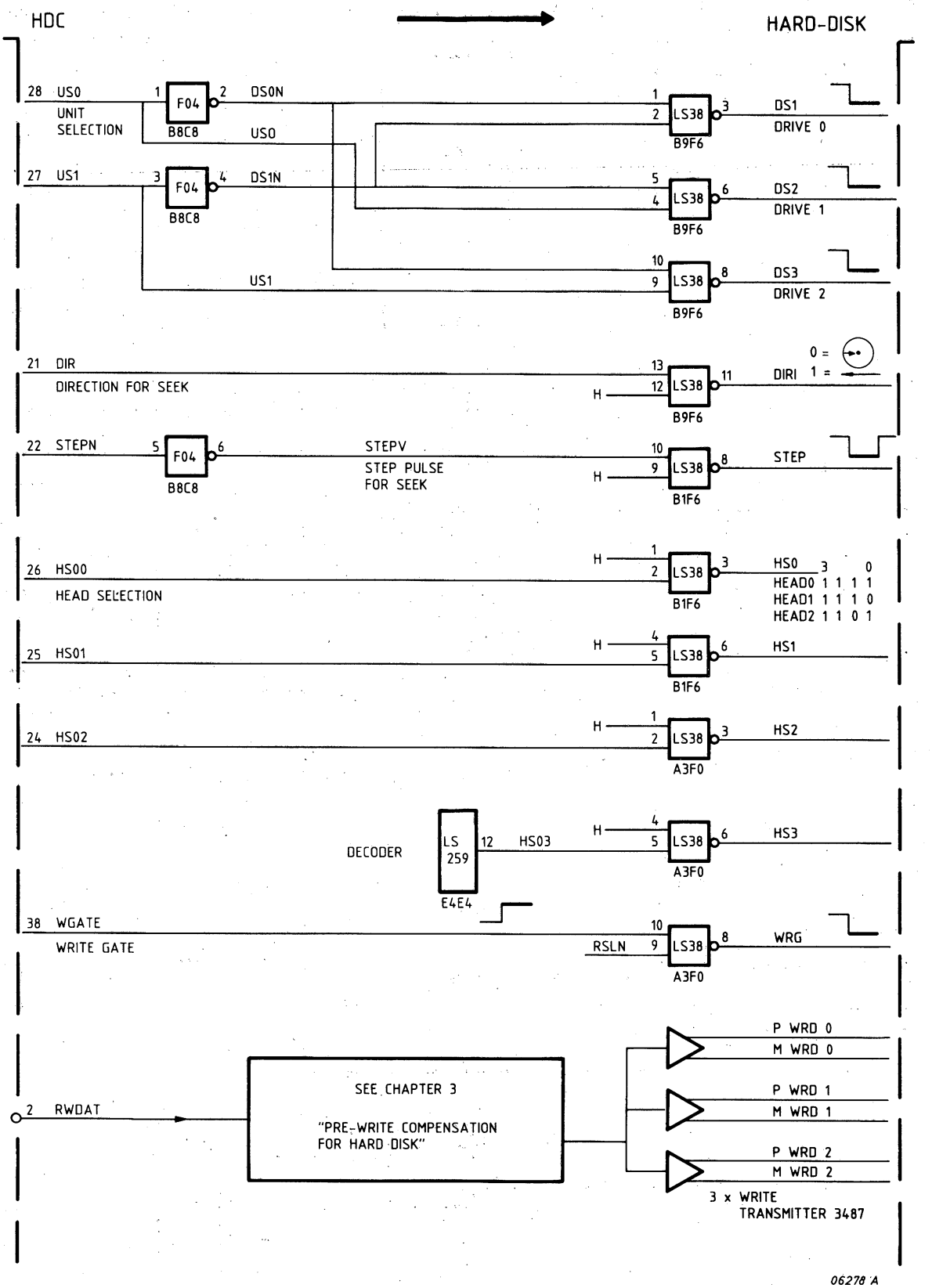


Figure 3.11a INTERFACE FDC TO/FROM FLOPPY DISK DRIVE

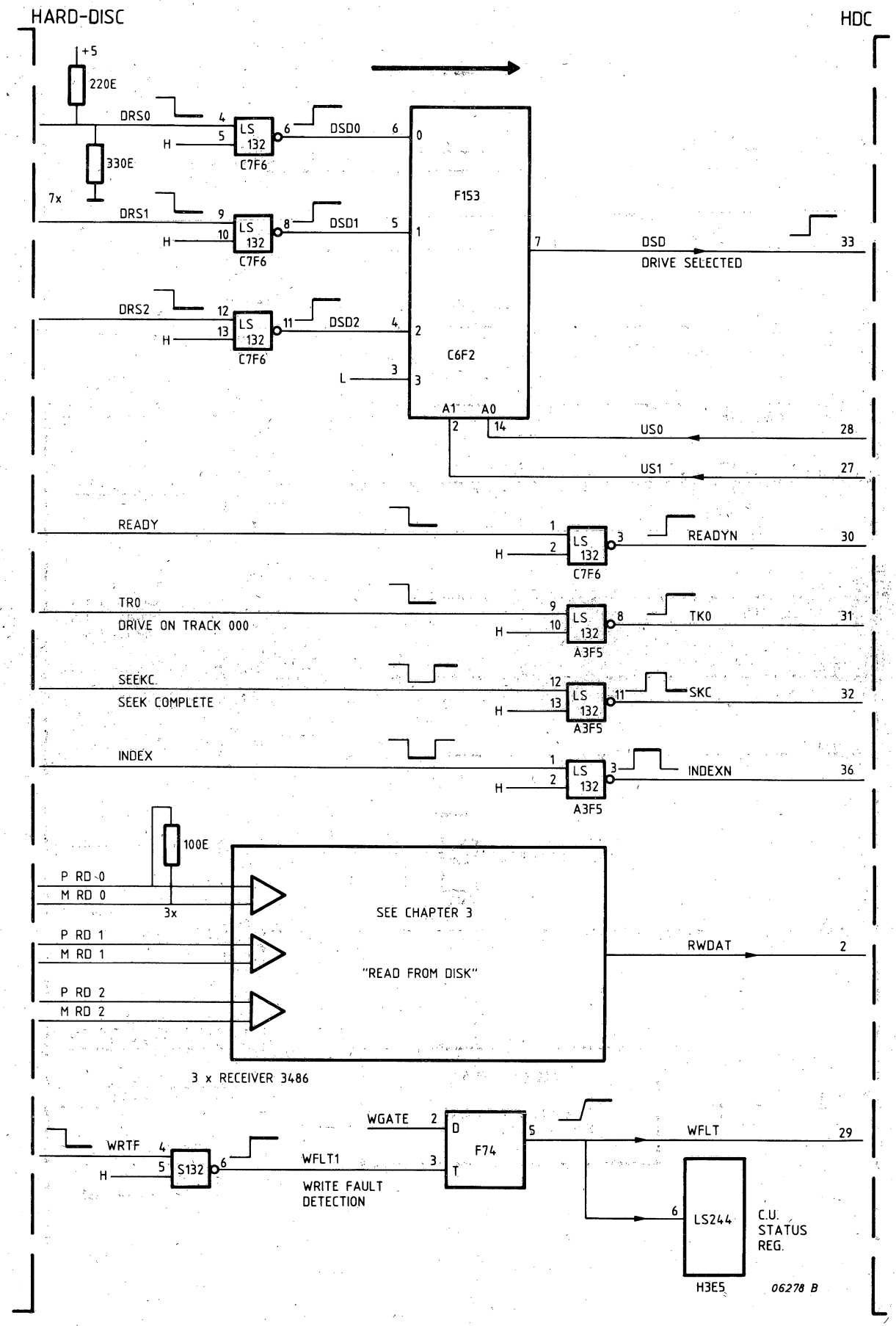


Figure 3.11b INTERFACE FDC TO/FROM FLOPPY DISK DRIVE

3.2.4 FLOPPY DISK CONTROL

3.2.4.1 FDC RELATION TO 8085, DMA AND LOCAL MEM.

What is described for the hard disk in part 3.2.3 also counts for the floppy disk part.
Here we have a floppy disk control (FDC) chip (765A) to handle the data transport as his internal sector count is zero (sector count number given during initialisation) the FDC requires a TC (Terminal Count) pulse to indicate that data transport is no longer necessary. Signal I55 is the interrupt line of the FDC to the microprocessor. For data transport to/from the FDC, channel 3 of the DMA-unit is used (contr. lines DREQ3 and DACK3).

3.2.4.2 INTERFACE, FDC TO/FROM FLOPPY DRIVES

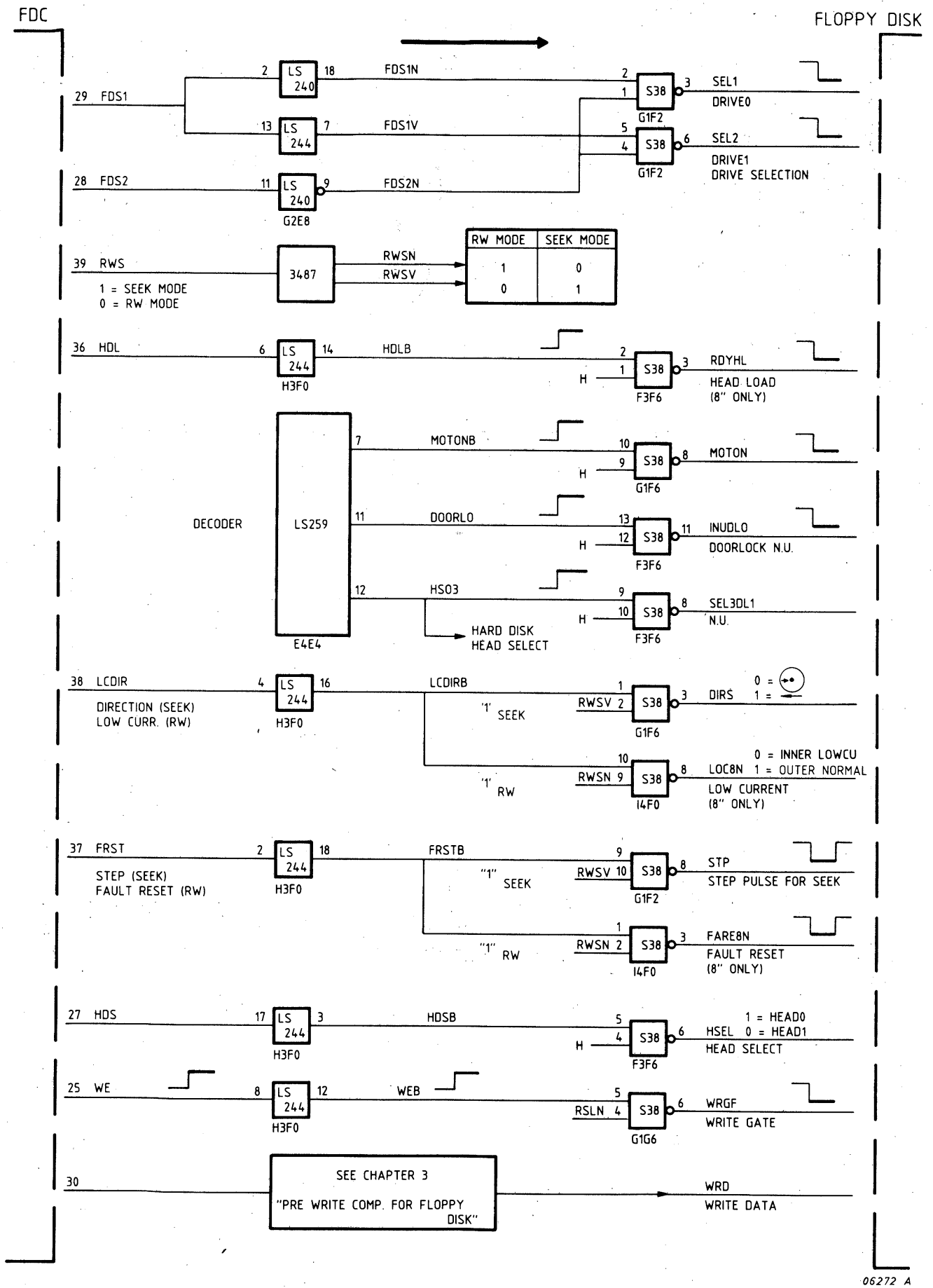


Figure 3.12a INTERFACE HDC TO/FROM HARD DISK DRIVES

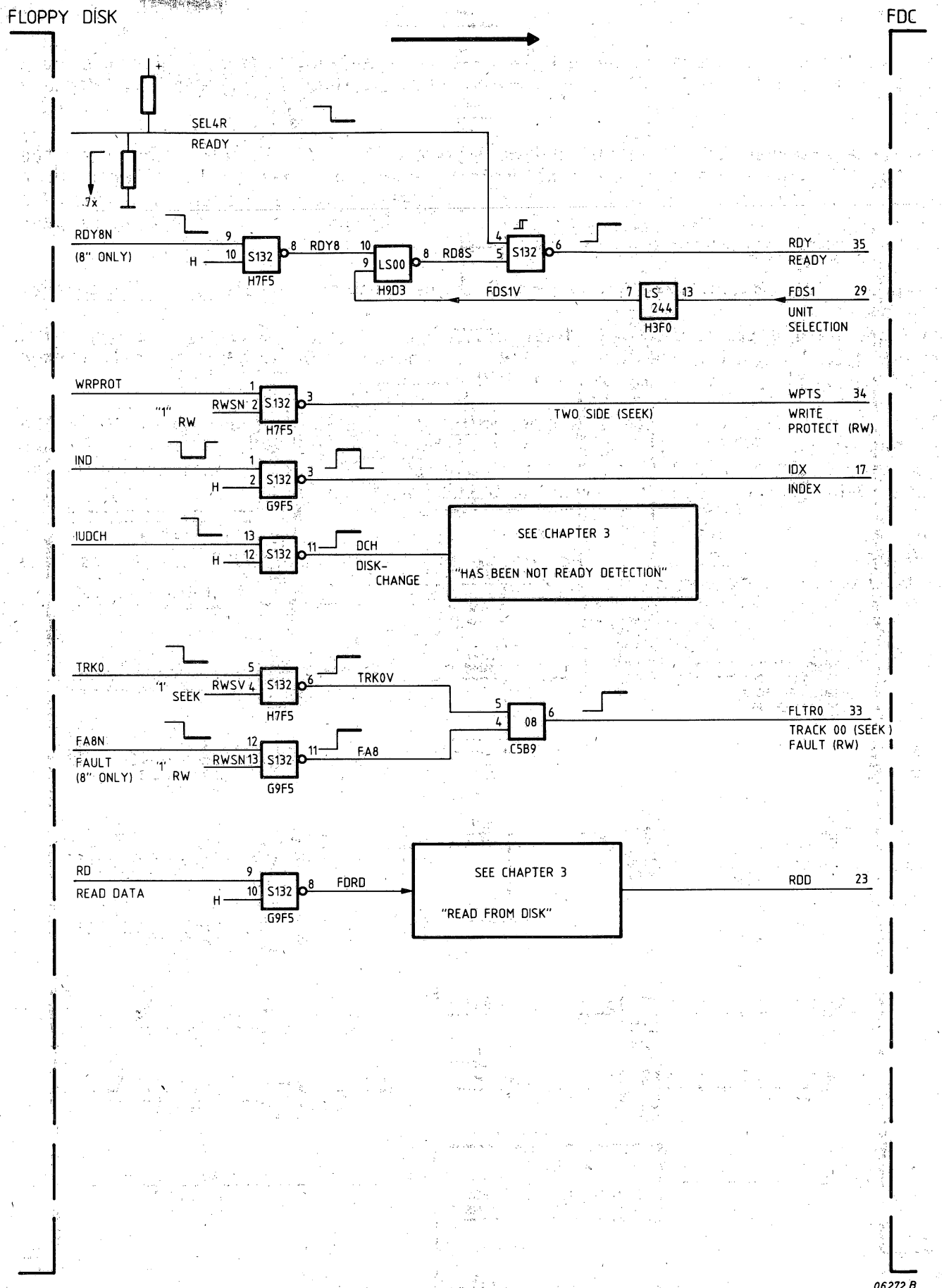


Figure 3.12b INTERFACE HDC TO/FROM HARD DISK DRIVES

3.2.5 DATA HANDLING FROM DISK

3.2.5.1 GENERAL

To and from the disks connected we have a serial data stream. For the hard disk this is only MFM-coded data, for the floppy drive as well MFM- as FM-coded data.

The decodation of this data is done by the Hard Disk controller (HDC) or by the Floppy Disk Controller (FDC). The FM/MFM coded data has to be offered in a special way to these controller chips, therefore a phase locked loop (PLL) is necessary. As this PLL is common for as well the hard- as the floppy-disk part it has to be switched over every time there is a change in drive type.

Figure 3.13 indicates how the serial drive data is handled by the several components.
For the hard disk we have the data PRD_X/MRD_X (x = 0,1,2 which corresponds with drive 0,1,2) entering the receiver 3486, its output (RD_X) enters the multiplexer F153 selected by the HDC by means of US0 and US1.

The selected data HDRD enters another multiplexer LS253; depending of RGATE the output of the LS253 (HDRDV) corresponds with HDRD or CL5 (PLLSYNC only important for other half of LS253). The last multiplexer (F157) selects only the hard disk data HDRDV or the floppy disk read data FDRD depending of HDFD.

So, RDC is the data which is offered to the PLL circuit. The PLL circuit delivers RDD and BF as data and window for the FDC and RWDAT and DBF as read data and R/W clock for the HDC.

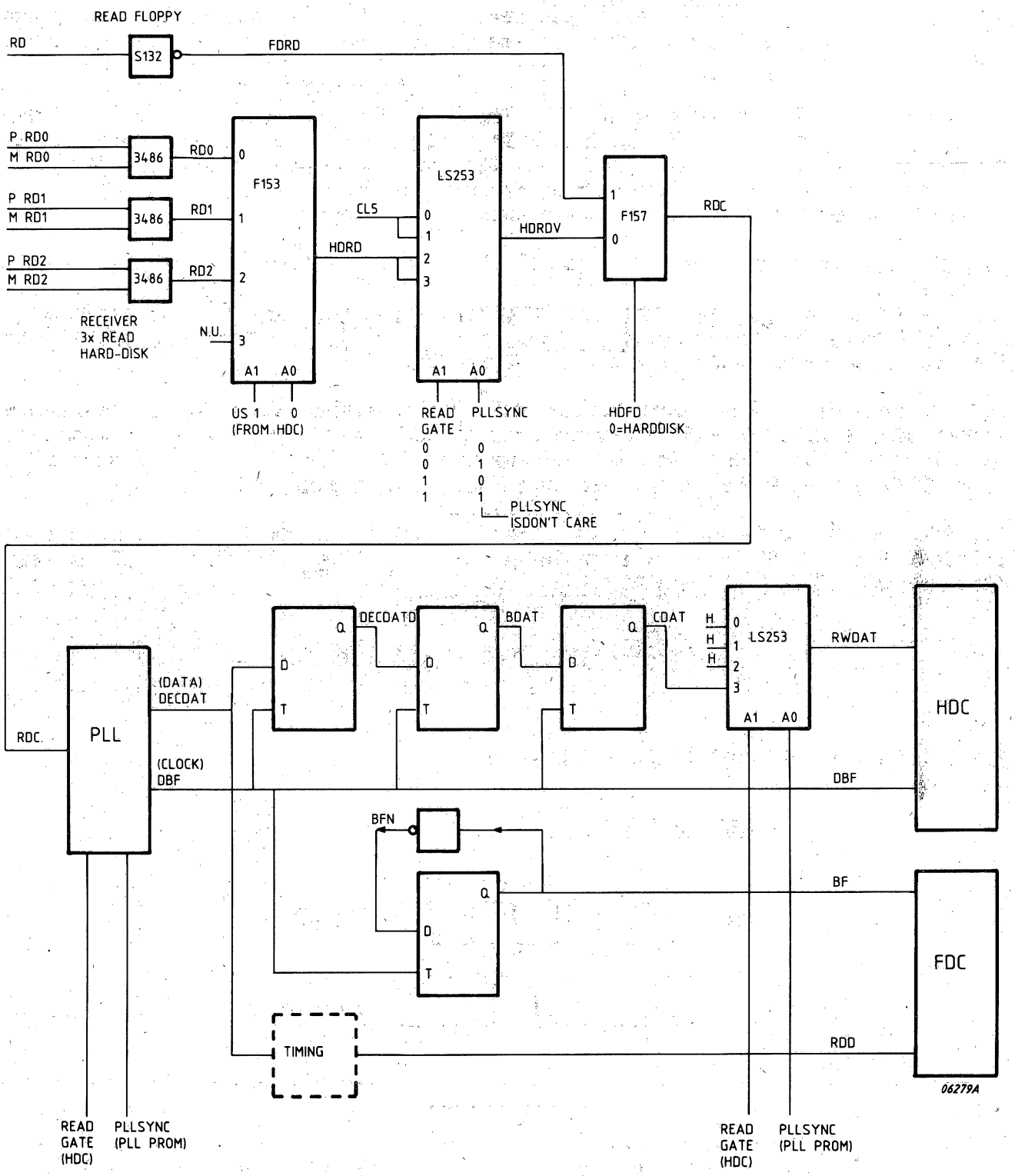


Figure 3.13 READ FROM DISK

3.2.5.1.1 FLOPPY DISK CONTROLLER BITCEL-TIME

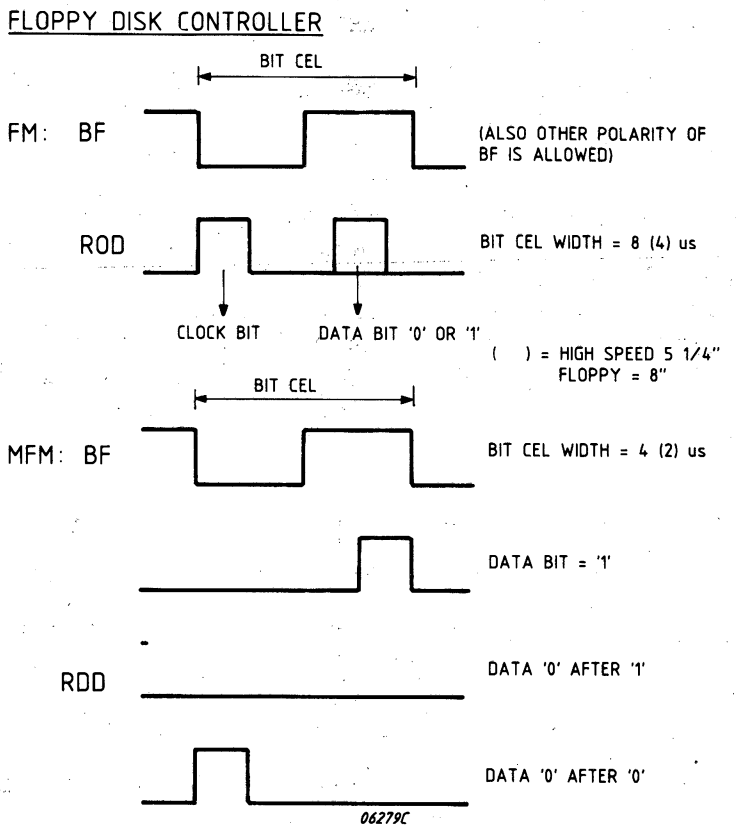


Figure 3.14 FDC BITCEL-TIME

3.2.5.1.2 HARD DISK CONTROLLER BITCEL-TIME

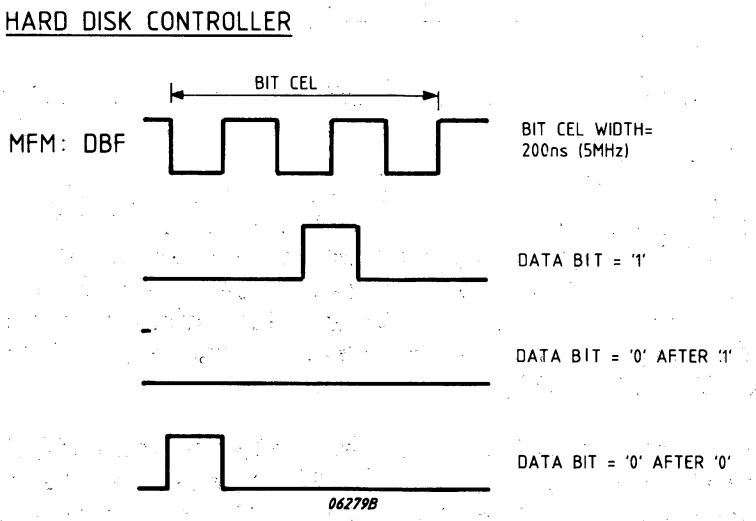


Figure 3.15 HDC BITCEL-TIME

3.2.5.2 READ FROM DISK

First the whole process will be described for the hard disk and after that the differences with floppy disk will be described.

3.2.5.2.1 DECODING AND PULSE SHAPING OF THE READ SIGNAL (SEE FIG. 3.16 AND 4.6)

The MFM encoded Read data signals are received on receiver 3486 on loc. *D5F5*. The three RDX signals are then multiplexed to signal HDRD.

Via multiplexers 74LS253 (*B1D7) and 74F157 (*C3C8*) signal RDC is obtained. During read from hard disk signal RGATE = 1 and for both Read and Write from or to hard disk signal HDFD = 0.

In order to decode the MFM coded signal RDC a phase locked loop is used to generate a clocksignal that is synchronous with RDC. In fact two clocksignals are generated being DBF and BF.
BF means bitfrequency while DBF means double bitfrequency. The nominal frequencies of DBF and BF are 10Mhz and and 5Mhz respectively.
The PLL is designed in such a way that the nominal using edge of DECDAT (buffered RDC) is in the middle of two rising edges of DBF (called data window). See figure 3.16.

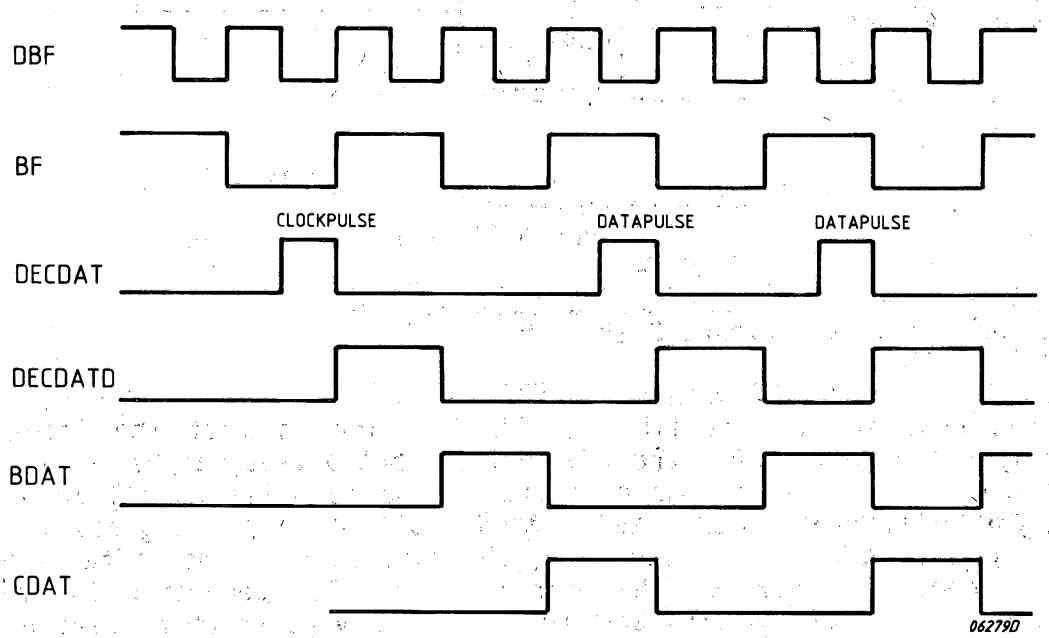


Figure 3.16 DECODING AND PULSE SHAPING OF THE READ SIGNAL

QDECDAT informed by two 74F74 flipflops such that WDECDAT :=1 after the rising edge of RDC and QDECDAT :=0 after the rising edge of DBF. If RDC was a data pulse (a '1') then DECDAT will coincide with the second half of a bittime (BF = 1), while if RDC was a clockpulse, then QDECDAT will coincide with the first half of a bittime (BF = 0). During the synchronization phase the edges of DBF and DECDAT can be very close to each other. Therefore DECDAT is clocked into a flipflop DECDATD (74F374*C8C7*).

DECTATD is clocked into flipflop BDAT and BDAT is clocked into flipflop CDAT. Now during the high level of BF signal CDAT represents the clockpulse and BDAT represents the data pulse of the foregoing bittime. These signals BDAT and CDAT are used to detect the preamble and the address marker and to detect whether the data bit is '0' or '1'. Signal CDAT is also fed to the R/WDATA input of the Hard disk controller via max. 74LS253 (*B1D7), but only when RGATE = 1 and PLLSYNC is '1', which means that the PLL is in synchronization during a read action.

Signal DBF is fed to the R/WCLK input of the HDC. Now that we know where DBF and DECDAT are used we shall described how DBF is generated.

The blockdiagram of the phase locked loop is given in figure 3.17.

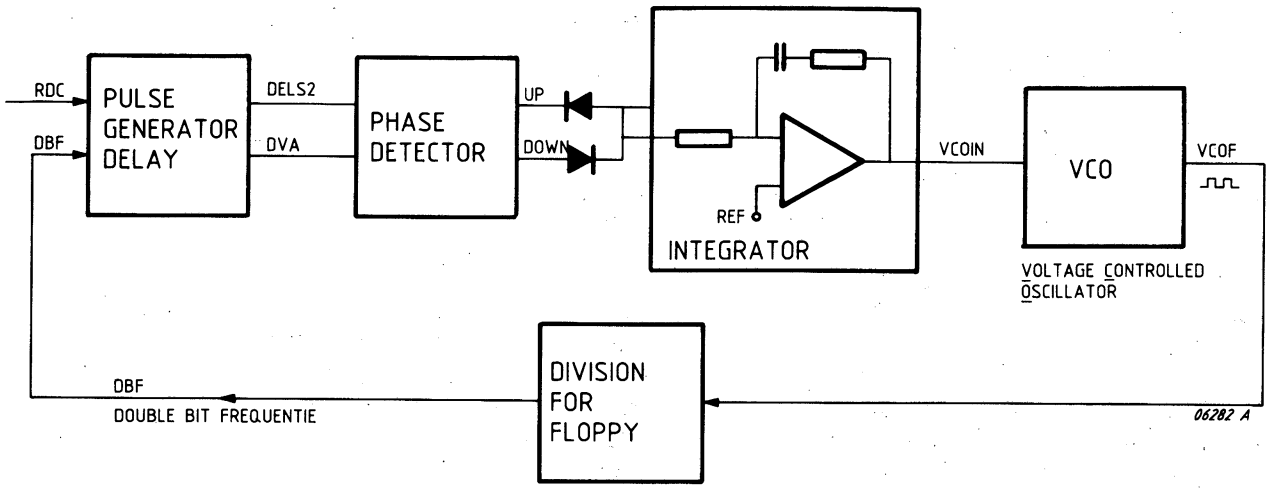


Figure 3.17 PLL

Division for floppy see figure 3.19.

One of the problems in designing a PLL for disk is that the incoming data (DECDAT) is not a continuous stream of pulses, but pulses can be in the first or in the second half of a bittime or there can be no pulse at all in a bittime. However, the phase comparator needs an edge of both input signals in order to generate an up or down pulse with a length equal to the time difference between these two edges. To overcome this problem the pulse generator is implemented that generates two signals. DVA and DELS2 that only pulse when there has been a DECDAT pulse (after synchronization is detected).

Signal DVA has a rising edge that corresponds to the rising edge of DBF. DVA is the output of a multiplexer on which either DECDATN or BF is selected.

BF is selected when the PLL in not yet in synchronization. Then the PLL must synchronize on an incoming data pattern of all zeroes (the preamble), which means a regular pattern of pulses in the first half of every bittime. So the frequency of BF will become equal to that of the incoming data (frequency synchronization). When the PLL is in synchronization the multiplexer 74F153 (*D3B9) switches from BF to DECDATN (only phase synchronization).

DECDATN has a rising edge that corresponds to the rising edge of DBF, but only when there is also a DECDAT pluse (DECDATN had the opposite polarity of DECDAT).

So, there will always be a pulse on both DVA and DELS2, although there can be a phase difference between the two rising edges. Depending on whether the rising edge of DVA is earlier or later than the rising edge of DELS2, a down or an up pulse is generated by the phase detector. The duration of this pulse is equal to the time difference between the two edges. The up and down pulses are integrated by the integrator and the integrated signal is input to the voltage controlled oscillator.

Up pulse lead to a higher frequency while down pulses lead to a lower frequency of the oscillator.
For hard disk signal VSOF is equal to signal DBF (via 74F157) on *C3C8*). So, now the loop is closed again. The integrator consists of an OP AMP with a filter. In fact there are two different filters, one for the hard disk and one for the much slower floppy disk.
The correct filter is selected by the switch on *B6B0* (see func. diagram 140-06). The oscillator is a 74LS628.

3.2.5.2.2 DELS2, DELAY FOR DECDAT PULSE

Signal DELS2 is a delayed DECDAT pulse.
I.c.o. 'MFM' the delay time is 1/4 bittime (nominal), while for FM coding the delay time is 1/8 bittime. This means that for MFM the rising edge of DECDAT will fall in the middle of two rising edges of DBF, while for FM the rising edge of DECDAT will fall on 1/8 bittime before the rising edge of DBF.
However, the FDC 765 wants the nominal data pulse to have a width of 30ns and to lay around the middle of the data window (DBF). Therefore an extra delay of 20ns is added.

So, the rising edge will lay 20 ns minus a propagation delay of a 74F08 before the middle of the window. A pulse of 30ns is formed by anding DECDAT with DEL30N and DELSN. See figure 3.18. The values of the delays are:

for hard disk : 50ns
for floppy X'3118' : 520ns
for floppy X'3114' : 1020ns

The 520 or 1020ns delays are selected by menas of a strap on *E0A5*.

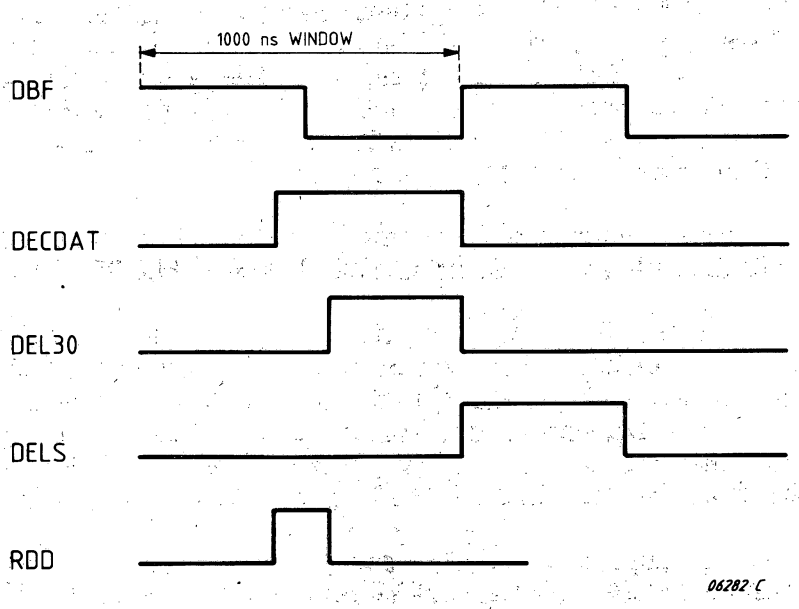


Figure 3.18 DELS, DELAY FOR DECDAT PULSE

3.2.5.2.3 FREQUENCY DIVISION FOR FLOPPY DISK (IN PLL)

I.c.o. floppy disk the frequency of the oscillator must be divided by 10 (MFM) or 20 (FM) to obtain DBF. The division is realised with a counter (74S163 on *A8C8*) plus a flipflop (74F74 on *B3C8*).

I.c.o. MFM code the counter is loaded with value 1100 and it counts to 0000 via 1101, 1110 and 1111.
This means that VCO2, being the most significant output of the counter, has a frequency that is a factor 5 lower than the frequency of VCOF.
VCO2 is divided by two on a flipflop (*B3C8*) with output VCO2D.
So, $VCO2D = \frac{VCOF}{10}$.

However, for the X3114 floppy disk drive, being a factor 2 slower, VCO2D must be divided by 2.
This is done on the flipflop with output VCO2DD.
By means of the straps on *B7C9* a selection is made between VCO2D and VCO2DD.
Signal VCO1 is then to the mux. (74F157 on *C3C*8) to selected i.c.o. floppy disk.

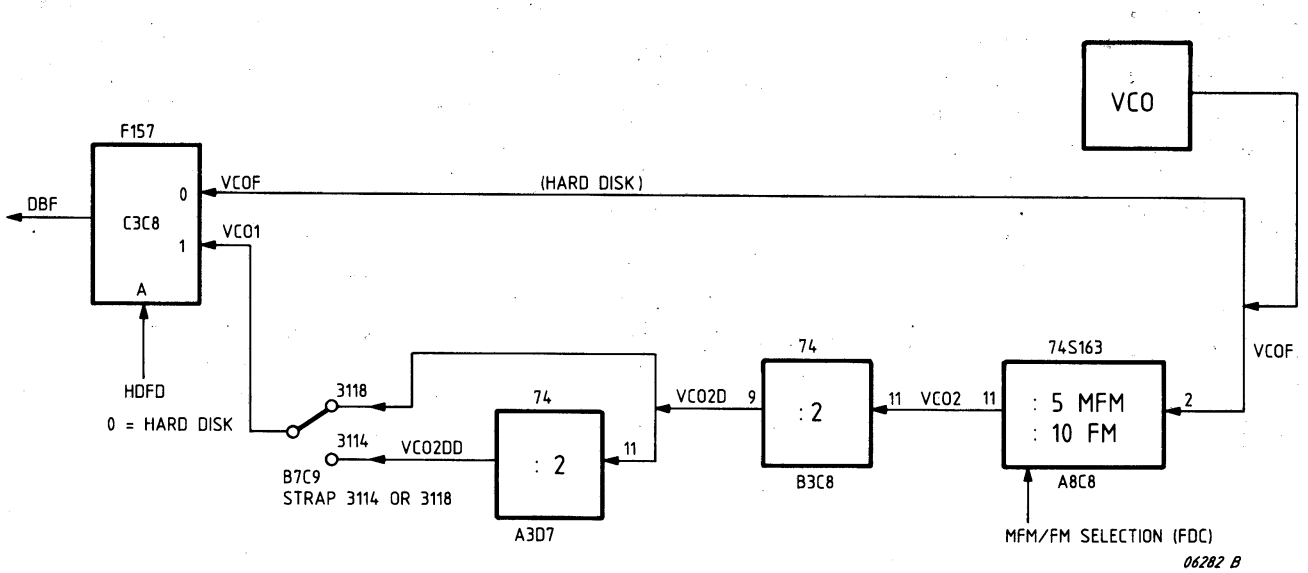


Figure 3.19 FREQUENCY DIVISION FOR FLOPPY IN PLL

3.2.5.2.4 PREAMBLE DETECTION

The preamble detection is done in the controller chips. However, the controller does not have a signal that indicates that the PLL is in synchronization. The PLL needs such a signal to switch from frequency synchronization to phase sychronization.

During frequency synchronisation BF is selected (74F153*D3B9*) to be compared with DELS2 while during phase synchronization signal DECDATN is selected.

To generate the synchronization signal PLLSYNC, a circuit is built that detects 16 zeroes and after that checks whether the address marker is following the zeroes. As soon as the 16 zeroes are detected PLLSYNC :=1 and PLLSYNC remains '1' until the controllers indicate the end of the read action (RGATE or VCO becomes 0) or when the circuit detects that no correct address marker is following the zeroes.

When no correct AM is found then PLLSYNC :=0 and the frequency synchronization and the search for a correct preamble + AM starts again. The 16 zeroes are detected by means of a CRC chip (9401) in the following way:

As long as input CWE of the 9401 is low, a '0' will be shifted into the internal 16 bit CRC register with every BF pulse. Signal BDAT is connected to the CWE input. BDAT = 0 indicates a zero bit. When 16 successive zeroes have been clocked into the 9401 then signal Q16ZN (the ER output) becomes 0.

However, as soon as BDAT = 1 then a '1' is shifted into the 16 bit CRC register and now again 16 zeroes are needed to fill the CRC register with all zeroes.

When BDAT = 1 a '1' is shifted into the CRC register because the data output is inverted and then input to the data input of the 9401.
Internally the data output and the data input are exclusive ored and then input to the first flipflop of the shift register. The 9401 is present when both RGATE and VCO are zero, so it always starts with a CRC register that contains 16 ones. Q16ZN is one of the inputs of the PROM (82S185 on *D3C8*) for the AM detection.

3.2.5.2.5 ADDRESS MARKER DETECTION

Using signals HDFD, Q16ZF, MFM, BF, CDAT and BDAT the PROM is able to detect a correct AM. Therefore, also the 4 outputs are buffered (74F374) and fed back to the inputs of the PROM.

When Q16ZPN =0 the PROM returns to its initial state, which means that all four outputs are zero. When Q16ZPN :=1 the PROM starts to search for a correct preamble plus AM.

Signals DEC02:00 in fact from a counter that starts counting on the first '1' after Q16ZN has become '0'.
When the values of BDAT and CDAT correspond to the value of DEC02:00 then the value of DEC01:00 is incremented until 111 is reached, else DEC(03:00) are set to 0000 again.
When the value 1111 is reached, then this value is maintained, so PLLSYNC remains '1', until either RGATE or VCO is deactivated.

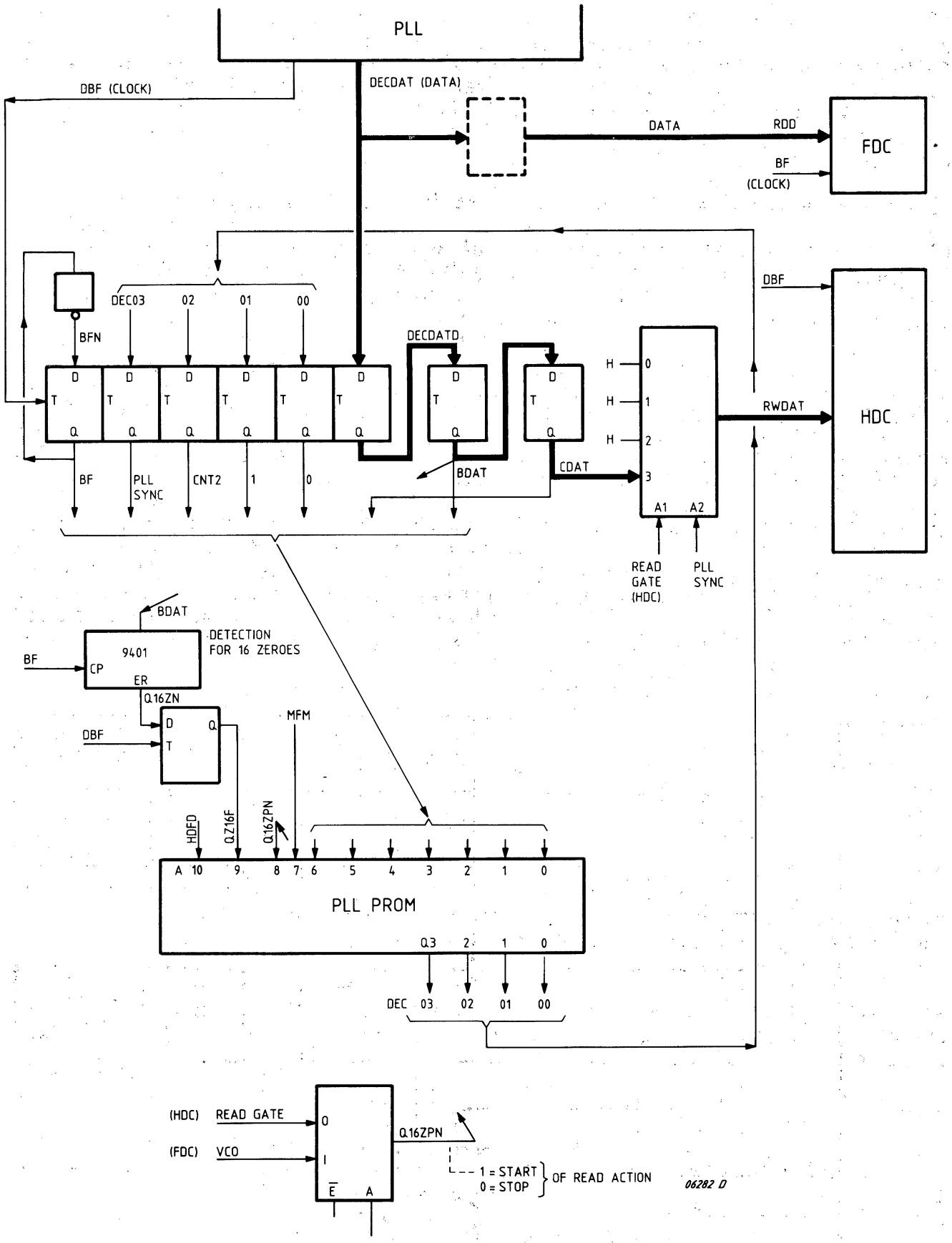


Figure 3.20 PLL PROM (SEQUENCER)

3.2.5.3 DATA TO DISK

3.2.5.3.1 WRITE ON DISK

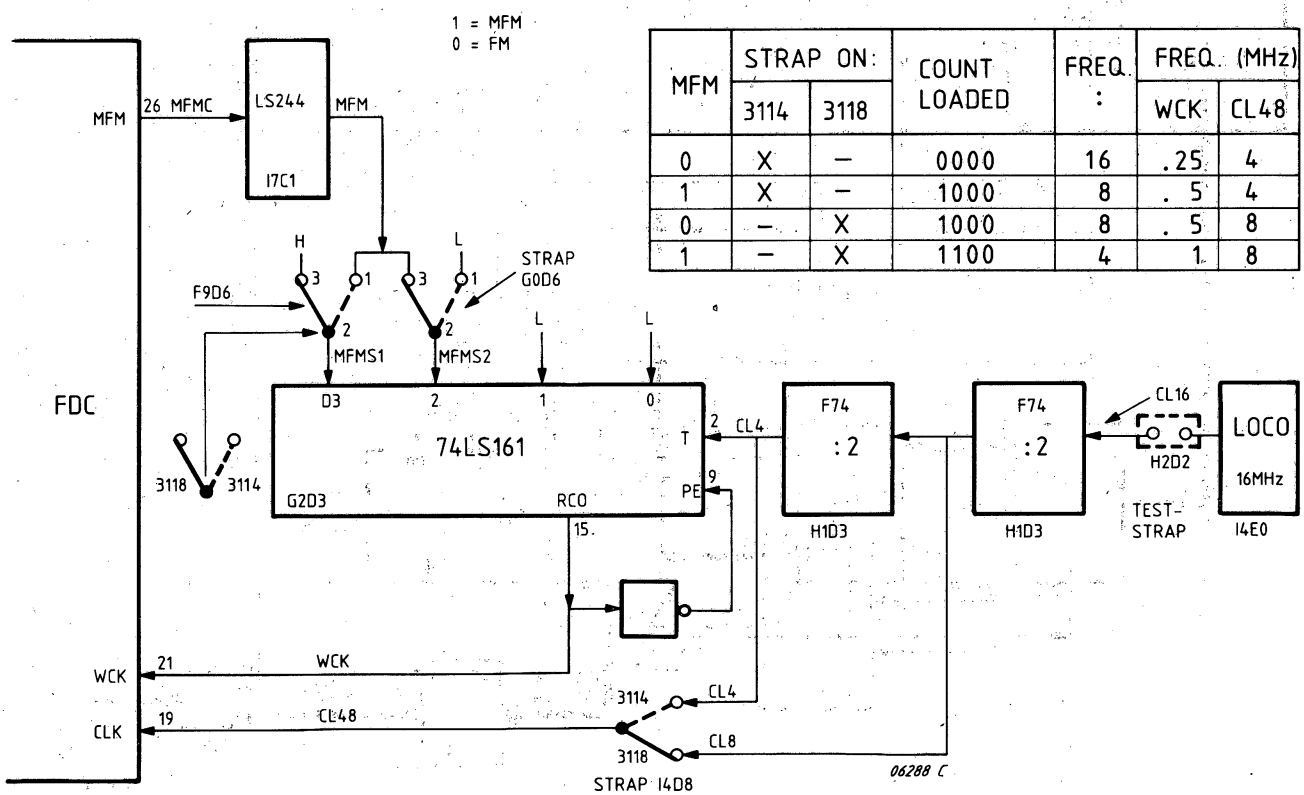
Almost all functions necessary for write on disk are implemented in the controllers (765 and 7261). Only the prewrite compensation is realized outside the controllers. For the floppy controller also a write clockpulse mut be generated.

3.2.5.3.2 WRITE CLOCK FOR FLOPPY DISK (SEE FUNCTION DIAGRAM 140-03).

The write clock must have a frequency of two times the bit frequency. This is obtained by dividing the output of LOCO (*14E0*). The frequency of this output is 16 MHz and it must be divided by 16 i.c.o. MFM on X3118 or X3138,
by 32 i.c.o. FM on X3118 or X3138,
by 32 i.c.o. MFM on X3114 and
by 64 i.c.o. FM on X3114

The signal CL16 is first divided by two flipflops giving an 8MHz signal CL8 and a 4 MHz signal CL4.
Depending on the drive type one of these signals is selected by a strap (*14D8) and input to the general clock input (CLK) of the 765.

Signal CL4 is used as clock input of a counter (74S161 on *G2D3*) that divides the frequency by 4, 8 or 16 depending on the signals MFMS1 and MFMS2. The division is realized by loading the counter with 12, 8 or 0 when it has value 16. The values of MFMS1 and MFMS2 depend on signal MFM and on the straps on *G0D6* and *F9D6*. For the X3114 on both straps pins 1 and 2 must be connected while for the X3118 and X3138 the pins 2 and 3 must be connected.



MFM	STRAP ON:		COUNT LOADED	FREQ. :	FREQ. (MHz)	
	3114	3118			WCK	CL48
0	X	–	0000	16	.25	4
1	X	–	1000	8	. 5	4
0	–	X	1000	8	. 5	8
1	–	X	1100	4	1	8

Figure 3.21 WRITE CLOCK FOR FLOPPY

3.2.5.3.3 WRITE CLOCK FOR HARD DISK

For the 7261 the R/WCKL pin is connected to signal DBF. This is possible because when RGATE =0 then the VCO is synchronized to signal CL5 being a 5 MHz signal that is obtained by dividing the 20 MHz output of a LOCO (*A3C9*). The CL5 signal is seleted on the input of the PLL by a multiplexer (*B1D7*).
(See Figure 4.6)

3.2.5.3.4 PREWRITE COMPENSATION FOR FLOPPY DISK (SEE FIGURE 3.22 AND 4.4)

The FDC has two outputs PS0 and PS1 that determine whether the write data pulse has to be given early, nominal or late. The meaning of these signals is as follows:

	PS0	PS1
Normal	0	0
Late	0	1
Early	1	0
Invalid	1	1

Prewrite compensation is only done for the inner tracks. This is selected by LCDIR, low current/Direction

LCDIR = 0 for outer tracks
= 1 for inner tracks

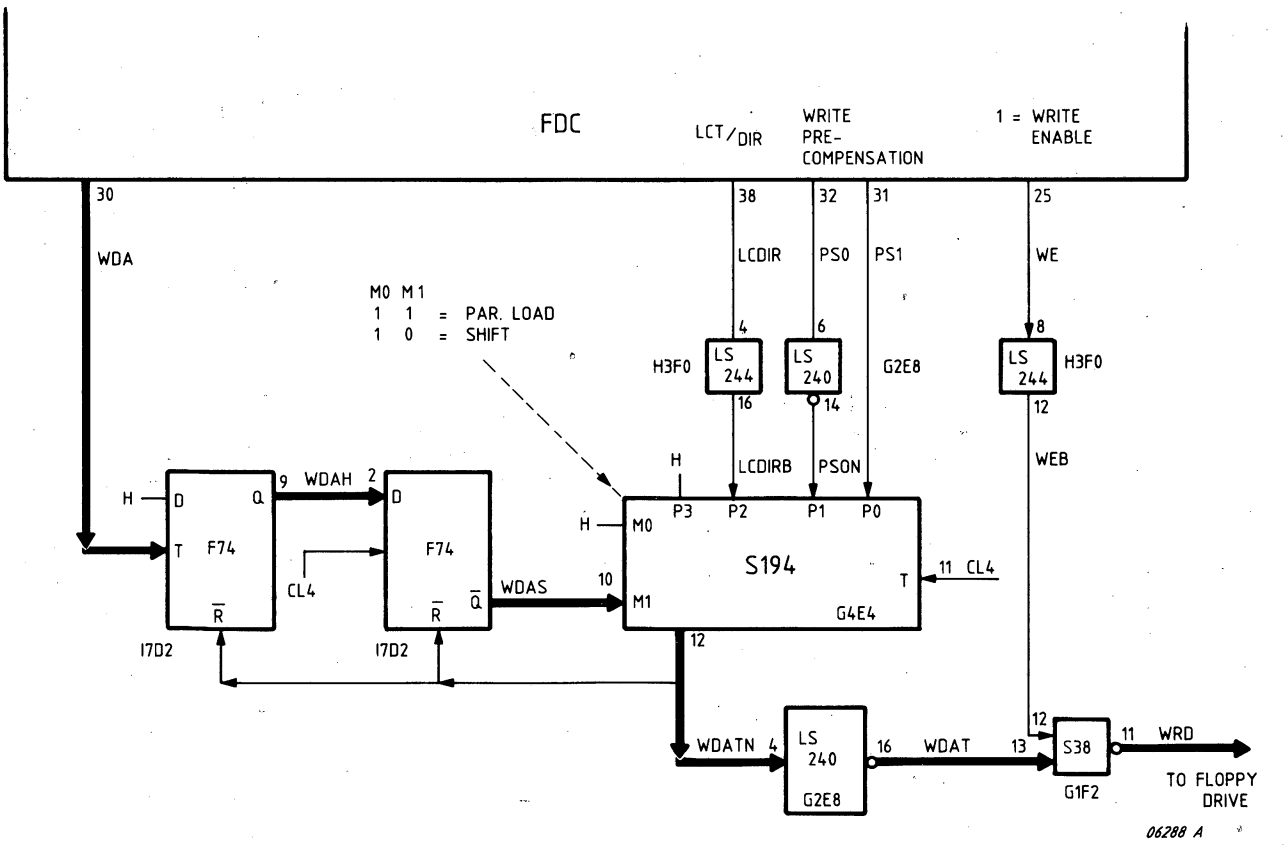


Figure 3.22 PREWRITE COMPENSATION FOR FLOPPY DISK

Another output (WDA) of the FDC indicates whether or not a pulse must be generated. On the rising edge of WDA flipflop WDAH is set. WDAH is clocked into flipflop WDAS on the rising edge of CL4. This is necessary because high to low transition of the M1 input of the 74S194 should only take place while the T input is high. The initial state before a WDA pulse is that WDAS = 1. This means that the shift register is loaded on every clockpulse (CL4). So, WDATN = 1 and flipflops WDAH remains 0 and WDAS remains 1.

When a WDA pulse comes, then WDAH :=1 and WDAS :=0 on the rising edge of CL4. So, on the following rising edge, as long as WDAS = 0 the shift register (74S194) will shift to the left.

As soon as a '0' is shifted into WDATN the flip-flops WDAH and WDAS will be reset causing WDAS :=1. Now we are back in the initial state. The number of CL4 pulses, needed to shift a '0' into WDATN, depends on the value that was loaded. When no precompensation is wanted, then signal LCDIRB = 0.
In table the values, loaded into the shift register are given and the number of CL4 pulses needed to get a '0' on WDATN depending on early or late.

	P3	P2	P1	P0	CL4
No comp.	1	0	X	X	1
Early	1	1	0	1	2
Normal	1	1	1	0	3
Late	1	1	1	1	4

In case of late a '0' is shifted into the the serial input of the shift register. From the table we see that the WDATN pulse comes one clock pulse earlier or later than normal, depending on PS0 and PS1.

3.2.5.3.5 PREWRITE COMPENSATION FOR HARD DISK (SEE FIGURE 3.23 AND 4.4)

For the hard disk the necessary prewrite compensation is only + or -10 ns. This time difference is obtained by delaying the RWDAT signal, after buffering in a 74F175 over 10, 20 or 30 ns and then selecting the appropriate delay output on a multiplexer with signals PCE and PCL (after buffering in the same 74F175) on the selection inputs. PCE=1 means EARLY, PCL=1 means LATE, PCE=0 and PCL=0 means NORMAL.

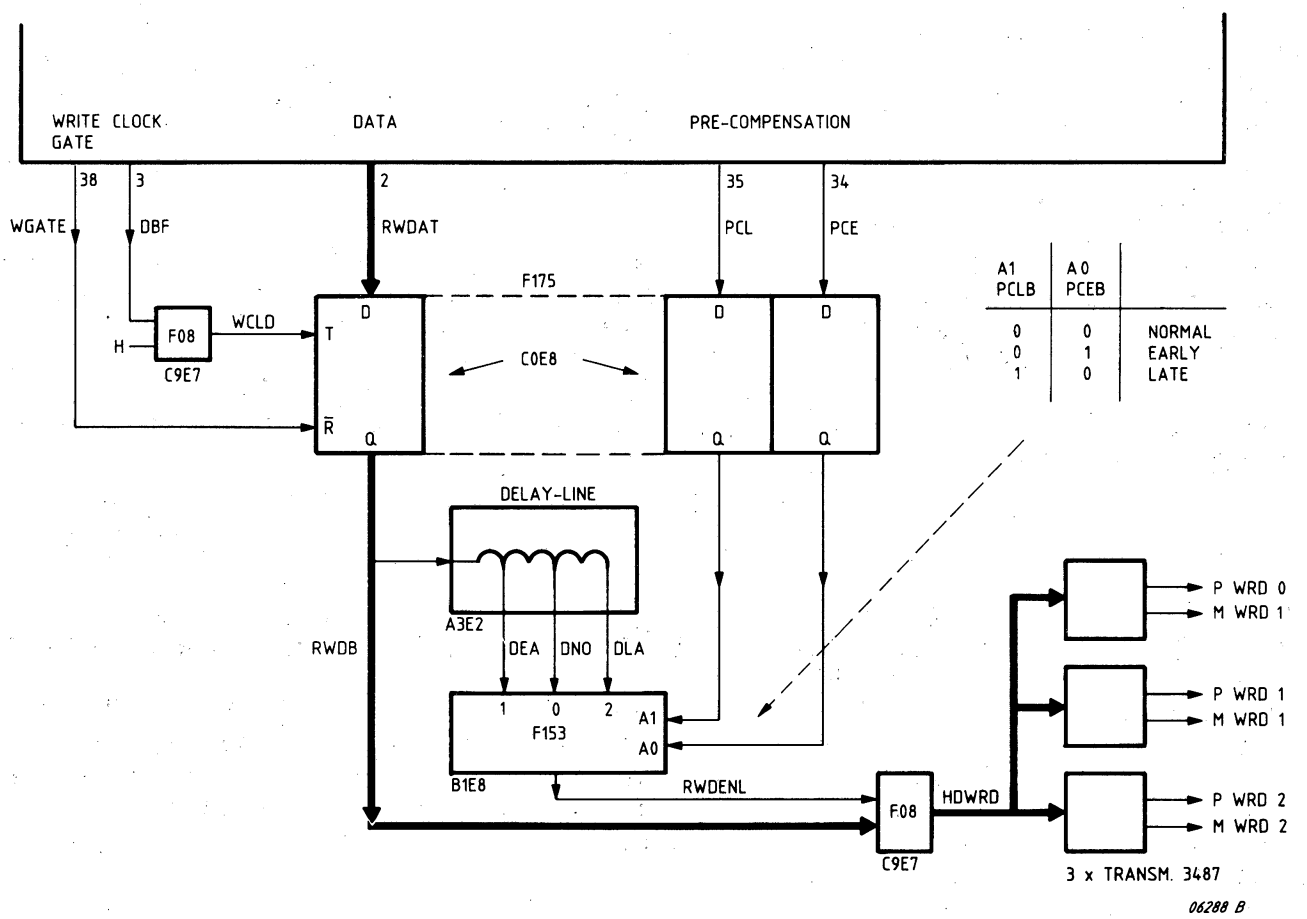


Figure 3.23 PREWRITE COMPENSATION FOR HARD DISK

3.2.6 UPL - PART (UPL-BUS)

The main items of the UPL - Part are:

a. Decoder (LS688), BUSLSI and IHC.
b. 3 output registers (LS374) to put an address on the UPL bus during a read or write to main memory.
c. In - and output data registers to store the data to and from the UPL data bus (BIO 00:15N).

3.2.6.1 DECODER (LS688), BUSLSI and IHC

The BUSLSI is used in the "CU mode". On TMPAN active and WRITE = 1 the start-FF of the BUSLSI is set as an indication a request has to be handled; TMPAN is the output of the cu-number decoder (LS688) where TMPN, MAD 10:15 and the cu-straps are the input conditions.

As the start-FF of the BUSLSI becomes active the microprogram performs the actions necessary and gives at the right time a release interrupt b.m.o. the BCI output of the IHC. The generated interrupt is reseted by the BUSLSI by RINTN as it receives a TMPAN and WRITE = 0.

The interrupt source code is loaded into the IHC by STIHCN (generated by the MPR); the code itself is applied by DB0:5 the mode by A5.

3.2.6.2 MEMORY ADDRESS REGISTER MAD

The 24 address bits (MAD 0:15, MADE 0:7) are loaded into 3 LS374 registers.
MAD 0:15 are loaded with A0:15 by the DMA-unit (8237); load command on these registers is MADLN from FPLA-2.
MADLN is a function of MEMWN, MEMRN generated by the DMA-unit and WRINT which indicate a write to main memory (WRINT=1) or a read from main memory (WRINT = 0). The most significant address part MADE 0:7 which are multiples of 64K are loaded by the MPR; address data is DB 0:7 and load pulse is LMADEN generated by decoder 74LS138. During the UPL bus cycle all 3 registers are enabled by EMADN generated by the BSULSI.

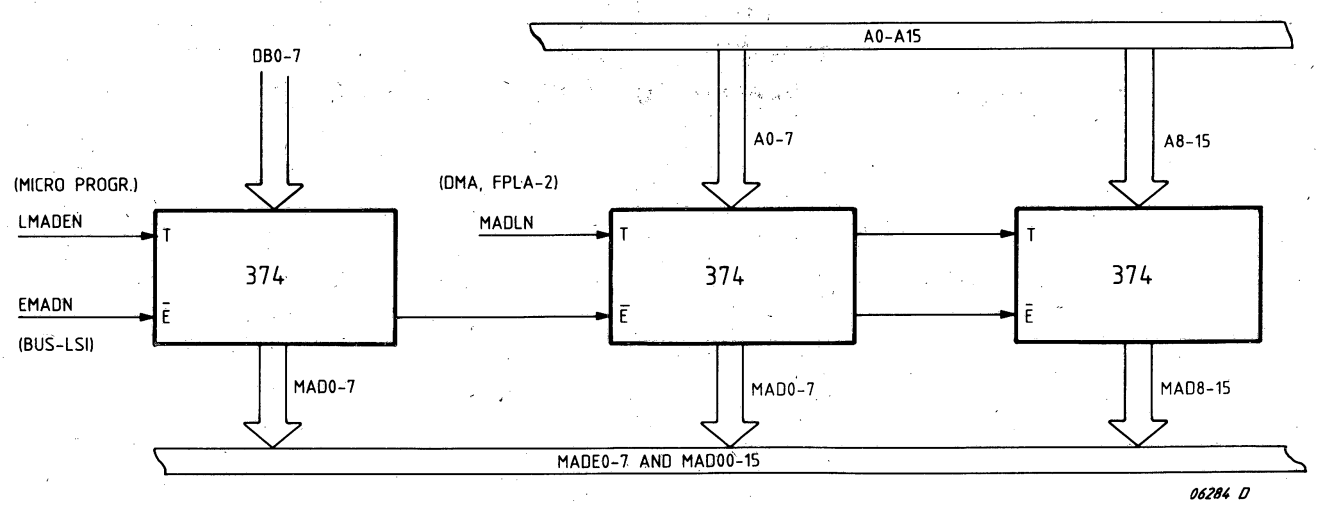


Figure 3.24 ADDRESS GENERATION OF UPL-BUS

3.2.6.3 IN-AND OUTPUT DATA REGISTER BIO

The data registers consist of two 74LS533 for sending data to the UPL-bus and two 74LS534 to fetch the UPL-data.
As the UPL-data bus is 16 bits wide (BIO 00:15N) and the internal databus in the cu 8 bits, we need separate control signal on the registers to transfer to/from local memory to/from main memory is done by the DMA-unit (8237).
In two DMA cycles the data to main memory is loaded into the output registers b.m.o. L07 and L815; during the UPL-databus b.m.o. EBon.
EBoN is generated by the BUSLSI circuit.
In case data is transfered from main memory to the control unit it is stored in the input registers (two 74LS534) during the UPL cycle by REQB.
REQB is generated by the BUSLSI circuit.
E07 enables the left character of the data on the internal databus and E815 the right character.

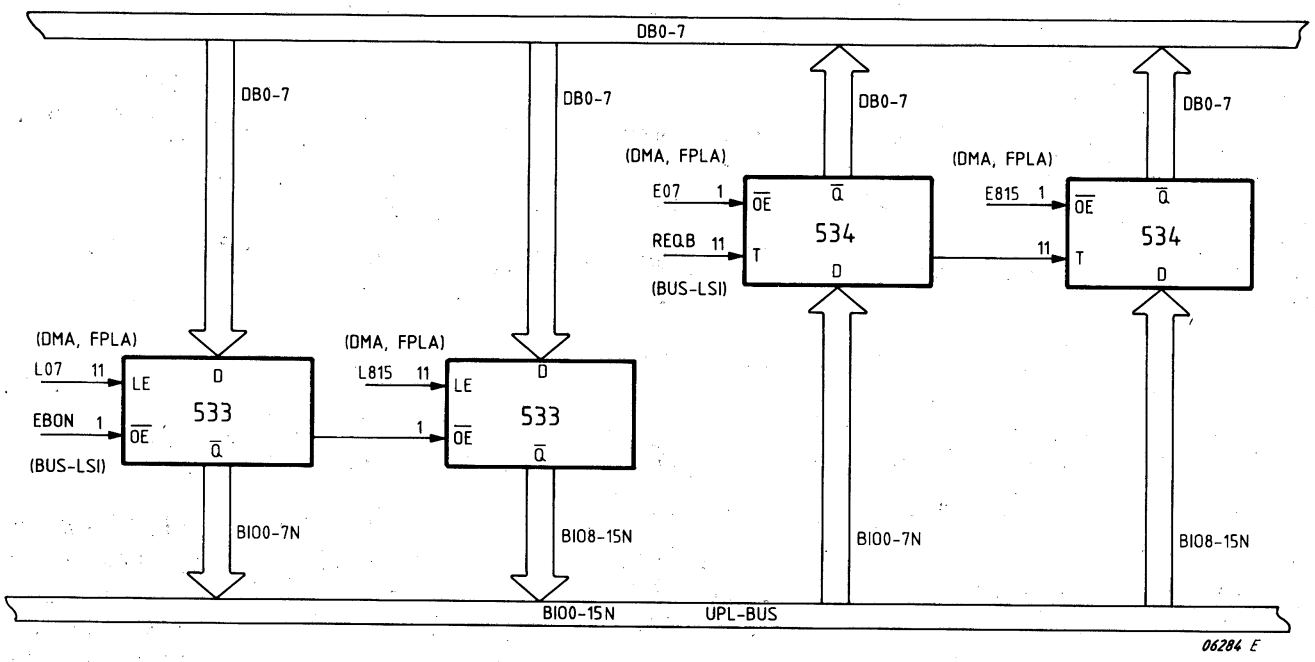


Figure 3.25 DATA IN/OUT REG. UPL-BUS

The table below indicated when L07, L815, E07 and E815 are active (low).

	AO	WRINT	AEN	MODEO	MEMWN	MEMRN
L 07	0	1	1	1	⊓	X
L815	X	1	1	1	⊓	X
E 07	0	0	1	1	X	⊓
E815	1	0	1	1	X	⊓

X = do not care
AEN = 1 DMA active
MODEO = 1 data transport between local memory and main memory
WRINT = 1 data transport to main memory
= 0 data transport from main memory.

Of BIO 00:15N is BIO 00:07N the left character (LC) and most significant byte and BIO 09:15N the right character (RC) and least significant part.

As MAD15 = 0 (in character mode) corresponds with LC and MAD15 corresponds with Ao, L07 and E07 are active as AO = 0.
They do not care of Ao for L815 means that as L07 is active and the LC is loaded, also L815 is active and so this LC is also loaded in the RC part.

Normally the following step is that Ao becomed "1", L815 is active again and the RC is loaded in the RC part. The reason that L815 is active at the moment L07 is also active is done for the case we operate in the LC has to take place by the RC part (see also part character operation).

INPUTS (PIN, NAME)										OUTPUT	
1	2	3	4	5	6	7	8	18	19		
WRINT	EOPN	AEN	MEMRN	MEMWN	MODEO	A13	AO	WDTIRN	TEST 1	PIN	NAME
										11	LL07
1	X	1	X	X	1	X	0	X	1	0	
										12	LL815
1	X	1	X	X	1	X	X	X	1	0	
										13	E07
0	X	1	⊓	X	1	X	0	X	1	⊓	
										14	E815
0	X	1	⊓	X	1	X	1	X	1	⊓	

X = Don't Care
TEST 1 = 1 is an enable for FPLA-1 (STRAP for "GENRAD")

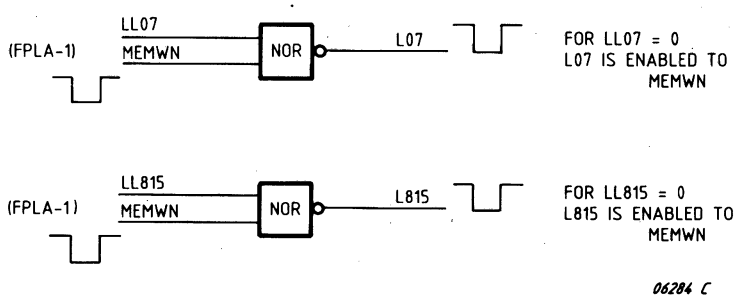


Figure 3.26 "DATA IN" REG. CONTROL

3.2.6.3 CHARACTER OPERATION

Below a table is given what has to happen during normal (word)-and character operation.

TABLE - Read, Write cycle modes

WRITE	CHA	MAD15	
0	0	X	READ WORD The memory bits are read on the BION lines
0	1	0	READ LEFT CHARACTER The most significant octade in memory is read on the least significant (Right hand octade) BION lines.
0	1	1	READ RIGHT CHARACTER The least significant octade in memory is read on the least significant (Right octade) BION lines
1	0	X	WRITE WORD The 16 bit word present on the BIO lines is written at the given address
1	1	0	WRITE LEFT CHARACTER The least significant octade on BIO lines is written on the most significant octade in memory
1	1	1	WRITE RIGHT CHARACTER The least significant octade on BIO lines is written on the least significant octade in memory

With the hardware indicated below and the fact that the output registers are loaded as described before (LC also is RC as L07 is active) character and word operation is done automaticly.

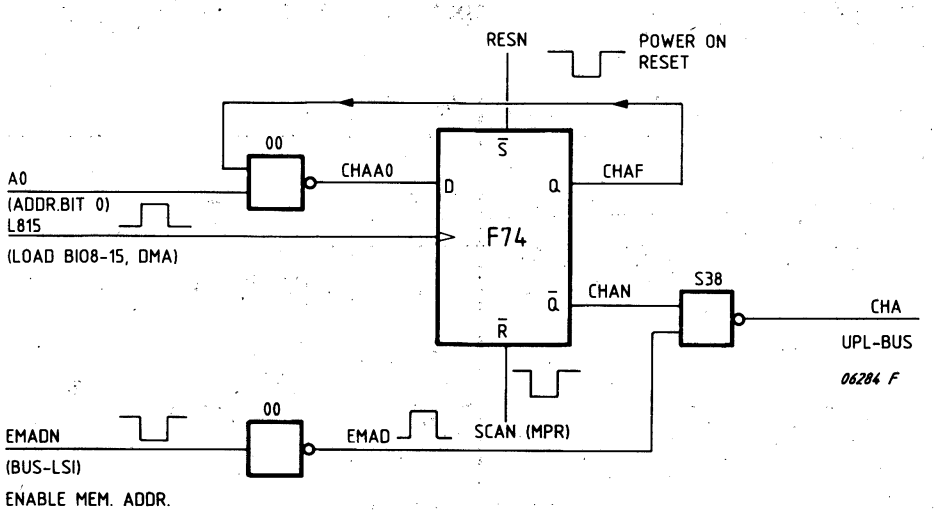


Figure 3.27 CHAR. FF UPL-BUS

During EMADN (generated by BUSLSI) CHA is enabled on the UPL-bus. The value of CHA is during data transport only depended of Ao and L815. Before data transport is started the F74 is reseted by SCHAN (MPR).

INITIALISE

SCHAN	CHAF	Ao	CHAAo	CHAN	CHA
0 ⟶	0	X	1	1	0*

* = when enabled
0 = word mode

WRITE WORD(S):

L07	L815	Ao	LC-Register	RC-Register	CHA	
		0	LC	LC	1	1st. DMA CYCLE
-		1	LC	RC	0	2nd. DMA CYCLE + BUS REQUEST

WRITE CHARACTER

L07	L815	Ao	LC-Register	RC-Register	CHA	
		0	LC	LC	1	1st. DMA CYCLE BUS REQUEST
-		1	LC	RC	0	1st. DMA CYCLE + BUS REQUEST

3.2.6.5 BUS REQUEST GENERATION

By giving a CLSTRN pulse to the BUSLSI circuit the control unit starts a bus request.
CLSTRN is generated in FPLA-1 with the input conditions as indicated below.

AEN	MODEO	Ao	WRINT	EOPN	MEMWN	MEMRN	CLSTRN
0	X	X	X	X	X	X	1
X	0	X	X	X	X	X	1
1	1	1	1	X	⌐⌐	X	⌐⌐
1	1	0	1	⌐⌐	X	X	⌐⌐
1	1	1	0	X	X	⌐⌐	⌐⌐
1	1	0	0	X	X	X	1

This table means the following:

- A bus request is only started as the DMA-unit is active (AEN=1) and MODEO is set to '1' as an indication transport between LM (local memory) and MM (main memory) has to take place.
- WRINT determines a main memory read or write action.
  EOP and MEMWN corresponds with the MM-write action and MEMRN with the MM-read action.

As main memory read is always done in word mode CLSTRN is only generated as Ao=1.

Main memory write actions can be done in as well word as character mode; in word mode a request is generated every time Ao=1; if only one character has to be transfered the MEMWN action is taken over by EOPN generated by DMA-unit indicating that no more data has to be transfered.

INPUTS (PIN, NAME)										OUTPUT	
1	2	3	4	5	6	7	8	18	19		
WRINT	EOPN	AEN	MEMRN	MEMWN	MODEO	A13	AO	WDTIRN	TEST 1	PIN	NAME
										9	CLSTRN
1	⊓	1	X	X	1	X	0	X	1	⊓	
1	X	1	X	⊓	1	X	1	X	1	⊓	
0	X	1	⊓	X	1	X	1	X	1	⊓	

X = Don't Care
TEST 1 = 1 is an enable for FPLA-1 (STRAP for "GENRAD")

3.2.7 V.C.O ADJUSTMENT

Normal conditions, see figure 3.28.
B1A9 is present; control signal from Ampl. connected to FC (freg. control of VCO).
B0A9 is open; the 2 diodes gives a min. and max. clamping of the control signal.
B7D2 is present; output of VCO is connected to the card.

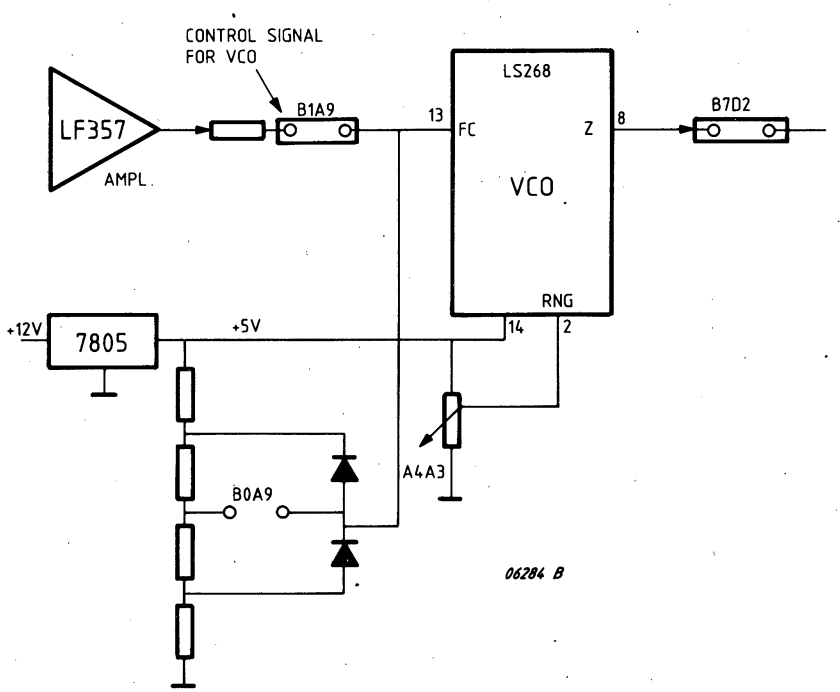


Figure 3.28 VCO, NORMAL CONDITIONS

Adjustment of V.C.O, see figure 3.29
Remove B1A9, Mount B0A9; the control signal is now a fixed voltage, independent of the ampl.
Remove B7D2, and connect a freg. meter.
Adjust the freg on 10 Mhz, this is the nominal freg. of the V.C.O
Set straps acc the normal conditions (figure 3.28)

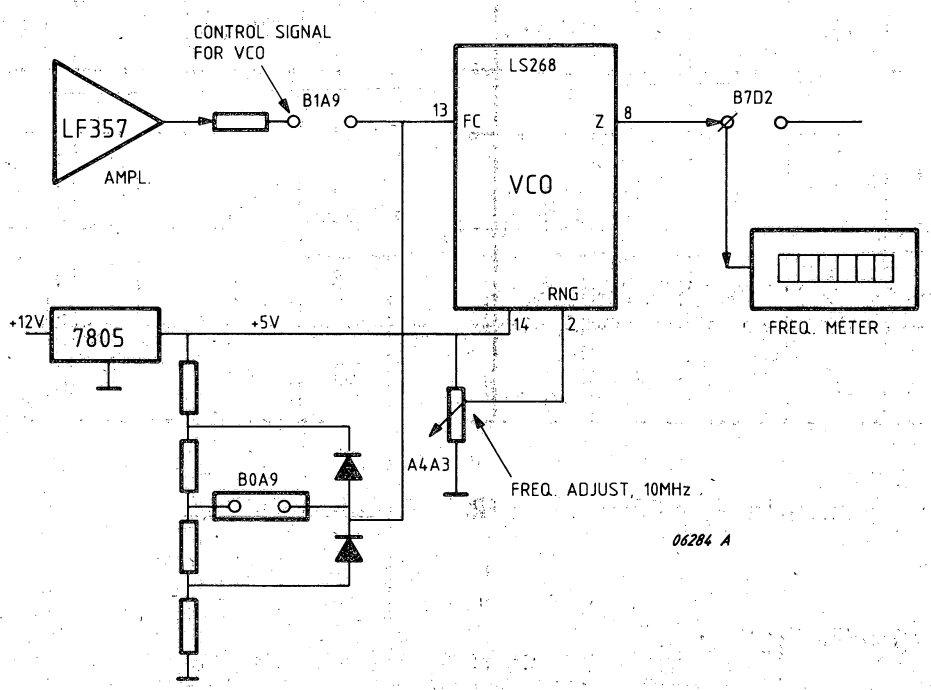


Figure 3.29 VCO, ADJUSTMENT CONDITIONS

4 DIAGRAMS

FIGURE	4.1	BLOCK DIGARM WDE	PAGE 4-3
	4.2	UPL PART - Bus LSI - C.U Address straps - C.U Address via backpanel - IHC LSI - Memory Address Interface - Data Bus Interface - Memory Address ext Latch - Memory Address Latch - Data Bus - Reset	4-5
	4.3	MICRO PROCESSOR CIRCUIT(S) - Clock generator - MICRO PROC 8085 - Hard Disk Controller 7261 - DMA - Floppy Disk Controller 765 - Floppy Write Clock - Write Compensation hard Disk - Address Latch 8085 - Tranceiver DB to from DBD - Address Latch DMA - EPROM - Ram - DTI Ram - Clock generation write Floppy	4-7
	4.4	HD-FD INTERFACE/DTI INTERFACE - 8 INCH Floppy option interface - Hard Disk Control Interface - Floppy Interface - Hard Disk Data 0/1/2 Interface - Hard Disk Read Data Receivers - Hard Disk Write Data Transmitters - Hard Disk Drive Selection - Hard Disk Read - Floppy Disk Change - Floppy Disk Write Data	4-9
	4.5	CONTROL PART - I/O MEM MAP Signals - Status Reg. - FPLA 's	4-11/12
	4.6	PLL DIGITAL PART	4-13
	4.7	PLL ANALOG PART - VCO - AMPLIFIER - NOT USED HARDWARE	4-15

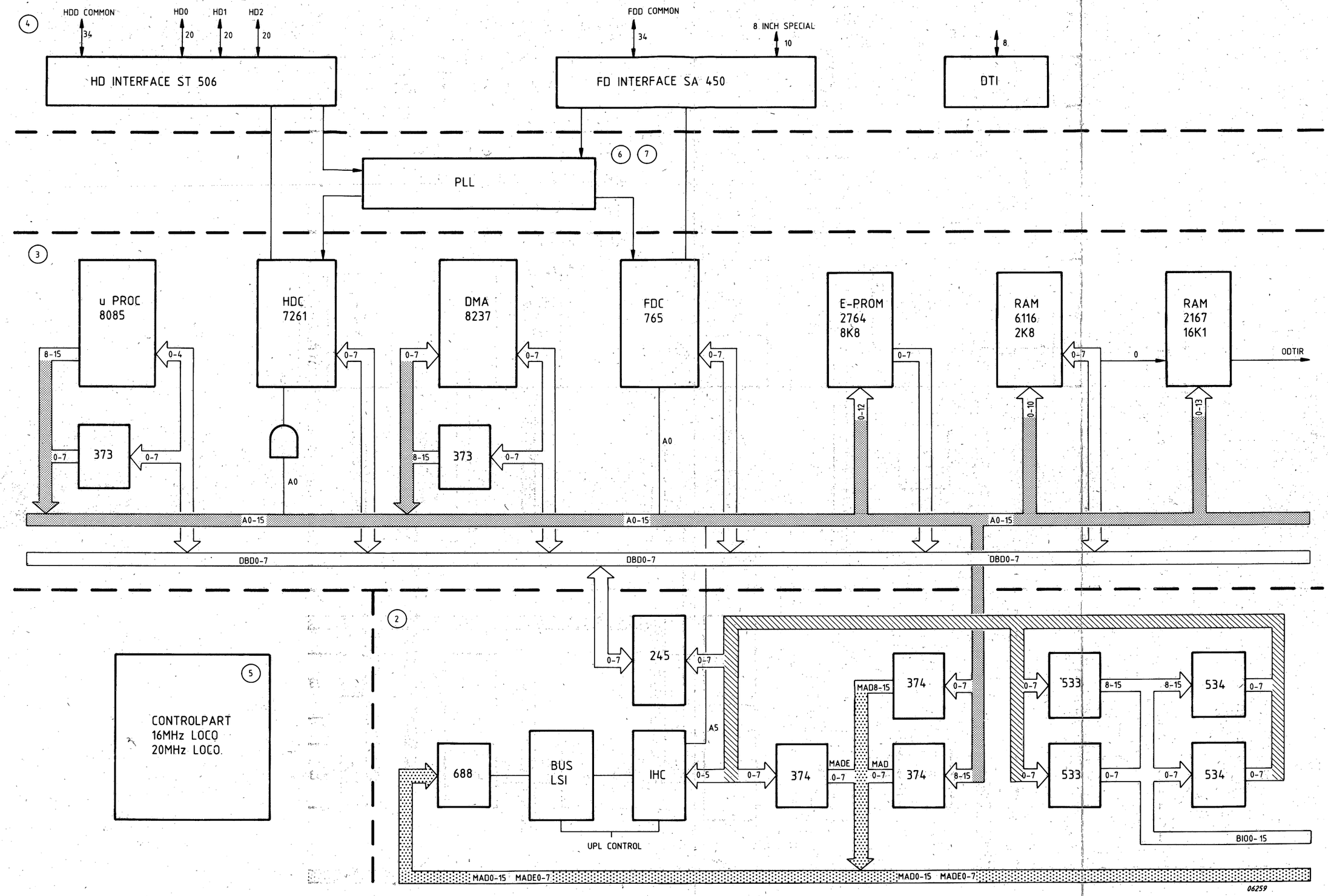
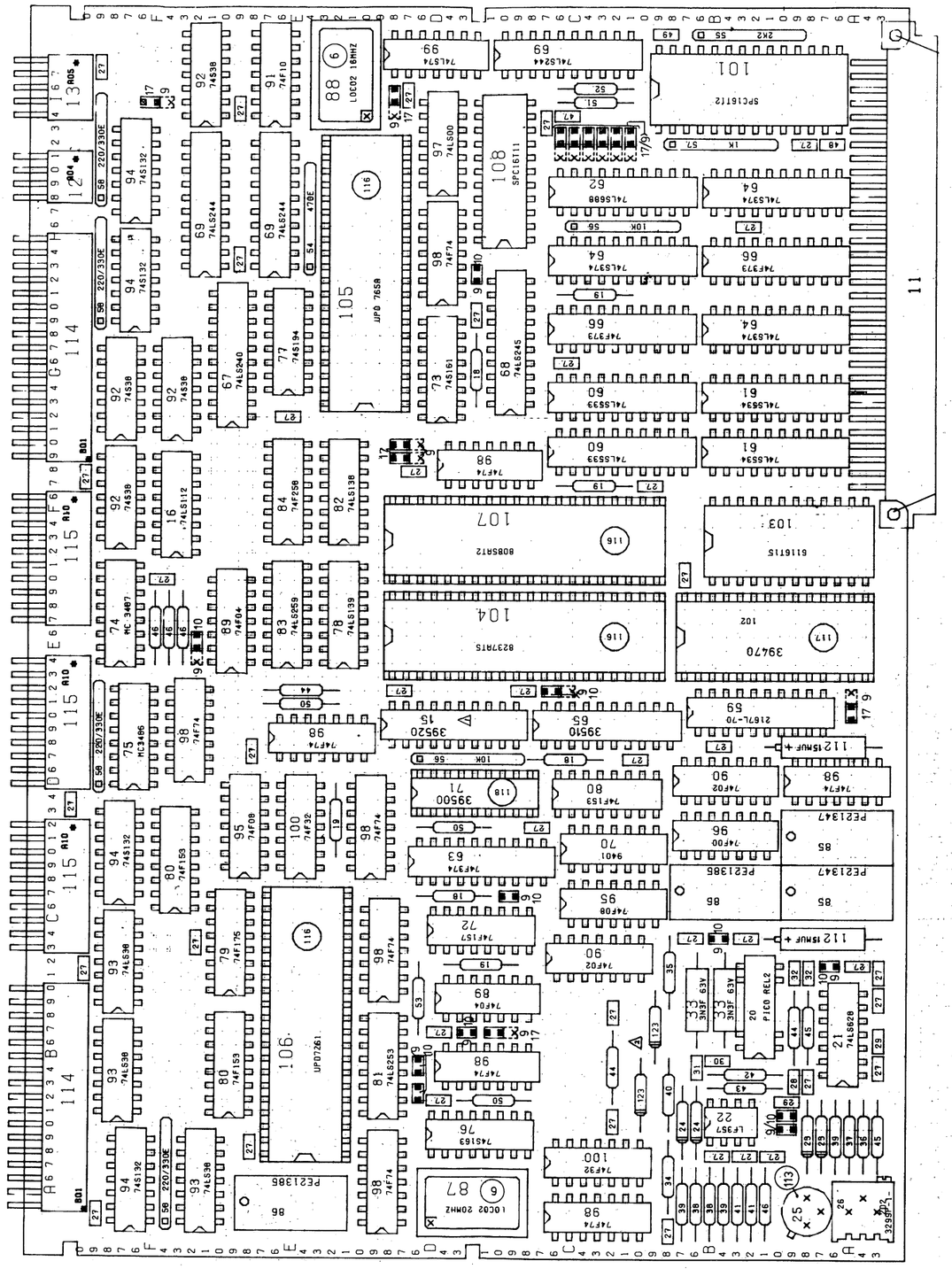


Figure 4.1 BLOCK DIAGRAM WDE



(1) BUS LSI

(2) CU ADDRESS STRAPS

(3) CU ADDRESS VIA BACKPANEL

(4) IHC LSI

(5) MEM ADDRESS INTERFACE

(6) DATA BUS INTERFACE

(7) MEM ADDR EXT LATCH

(8) MEM ADDR LATCH

(9) DATA BUS

(10) RESET

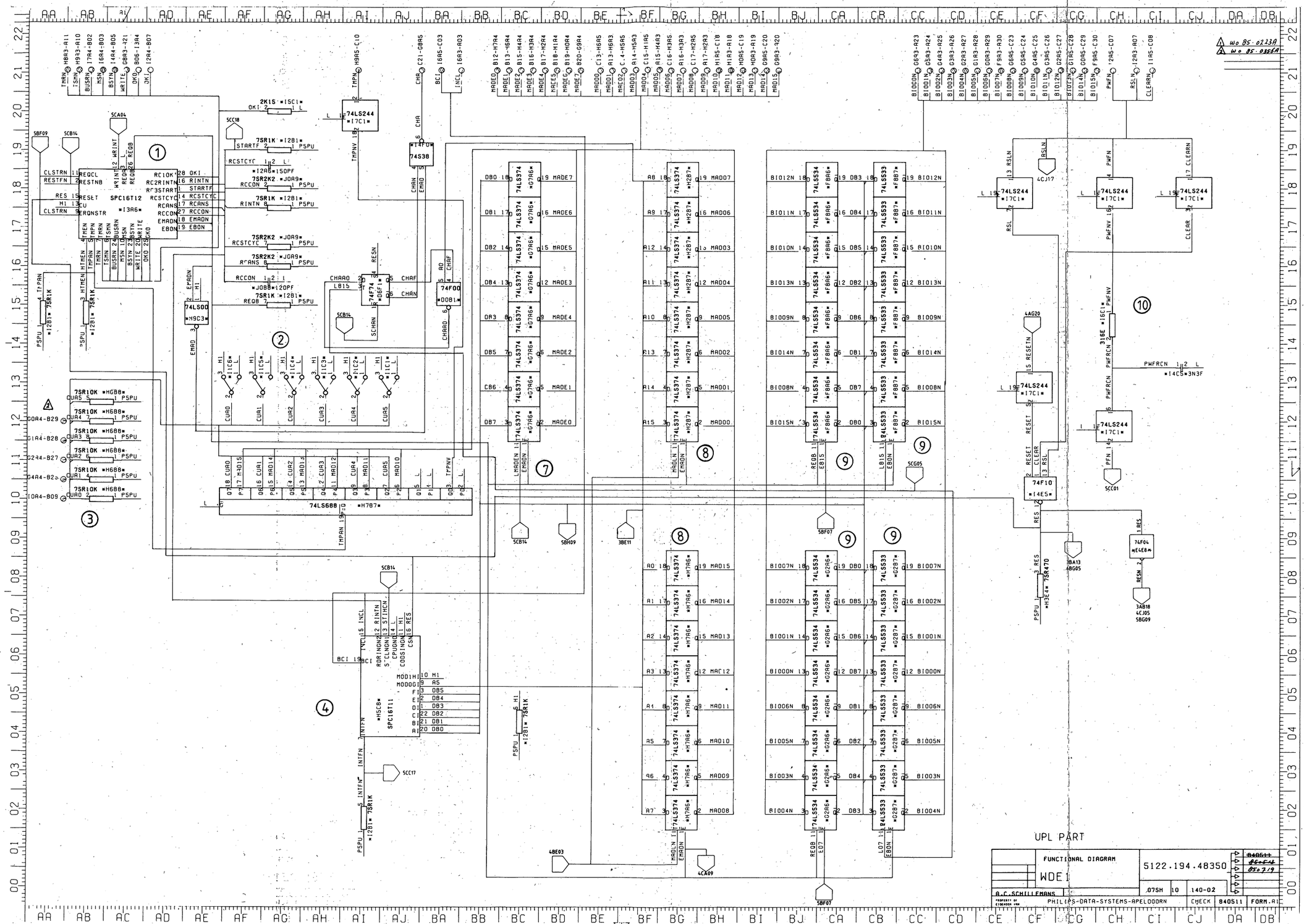


Figure 4.2 UPL PART

(1) CLOCK GENERATOR

(2) MICROPROC.

(3) HARD DISK CONTROLLER

(4) DMA

(5) FLOPPY DISK CONTR.

(6) FLOPPY WRITE CLOCK

(7) WRITE PRECOMPENSATION HD

(8) ADDRESS LATCH (8085)

(9) TRANSCEIVER DB — DBD

(10) ADDRESS LATCH (DMA)

(11) EPROM

(12) RAM, LOCAL MEMORY

(13) DTI RAM

(14) CLOCK GENERATOR FOR WRITE FLOPPY

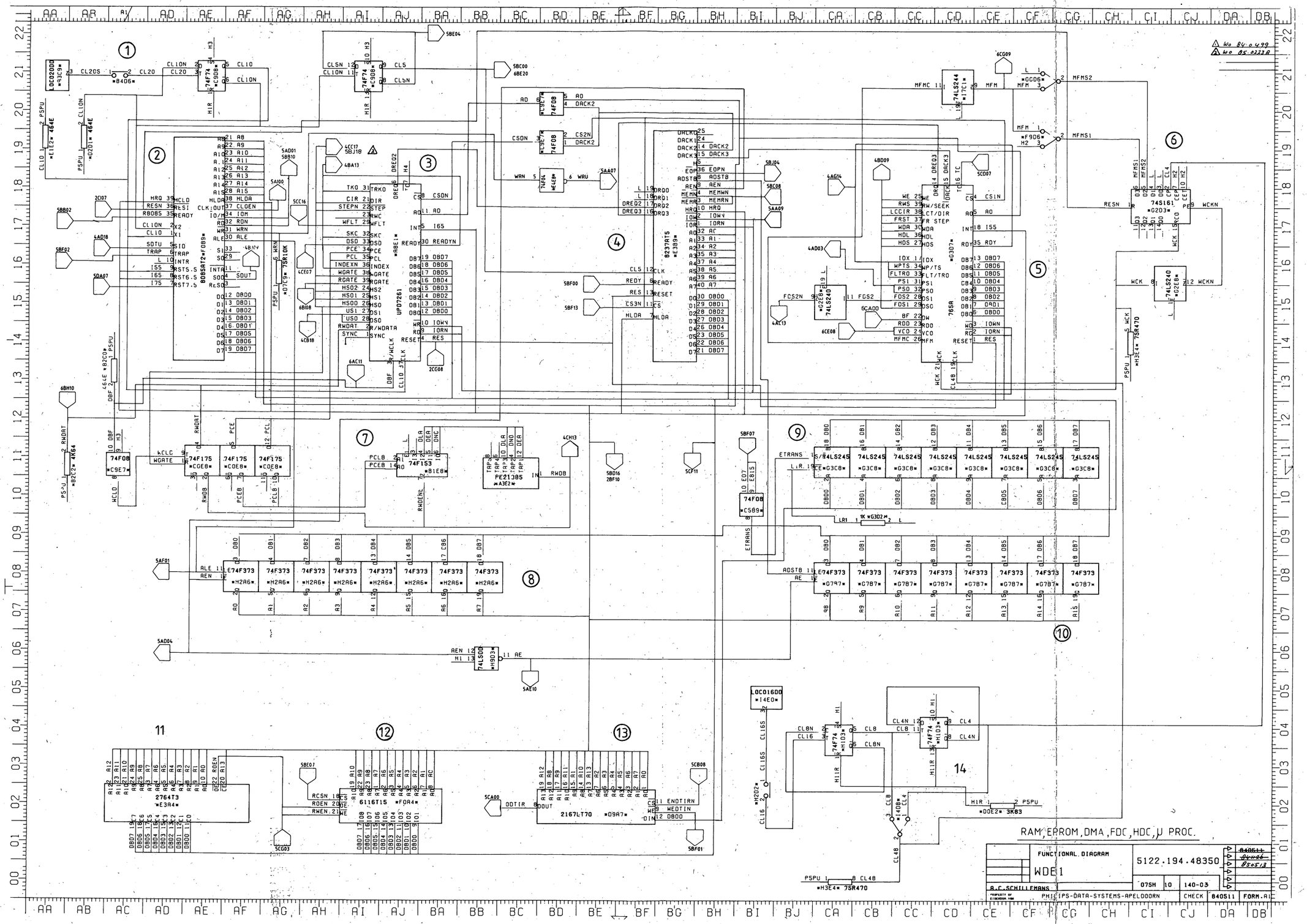


Figure 4.3 MICRO PROC. CIRCUIT(S)

(1) 8 INCh FLOPPY OPTION INTERFACE

(2) HD CONTROL INTERFACE

(3) FLOPPY INTERFACE

(4) HD DATA 0

(5) HD DATA 1

(6) HD DATA 2

(7) READ H.D. DATA RECEIVERS

(8) WRITE H.D. DATA TRANSMITTERS

(9) DRIVE SELECTED HD

(10) HARD DISK READ

(11) DISK CHANGE

(12) WRITE DATA FD

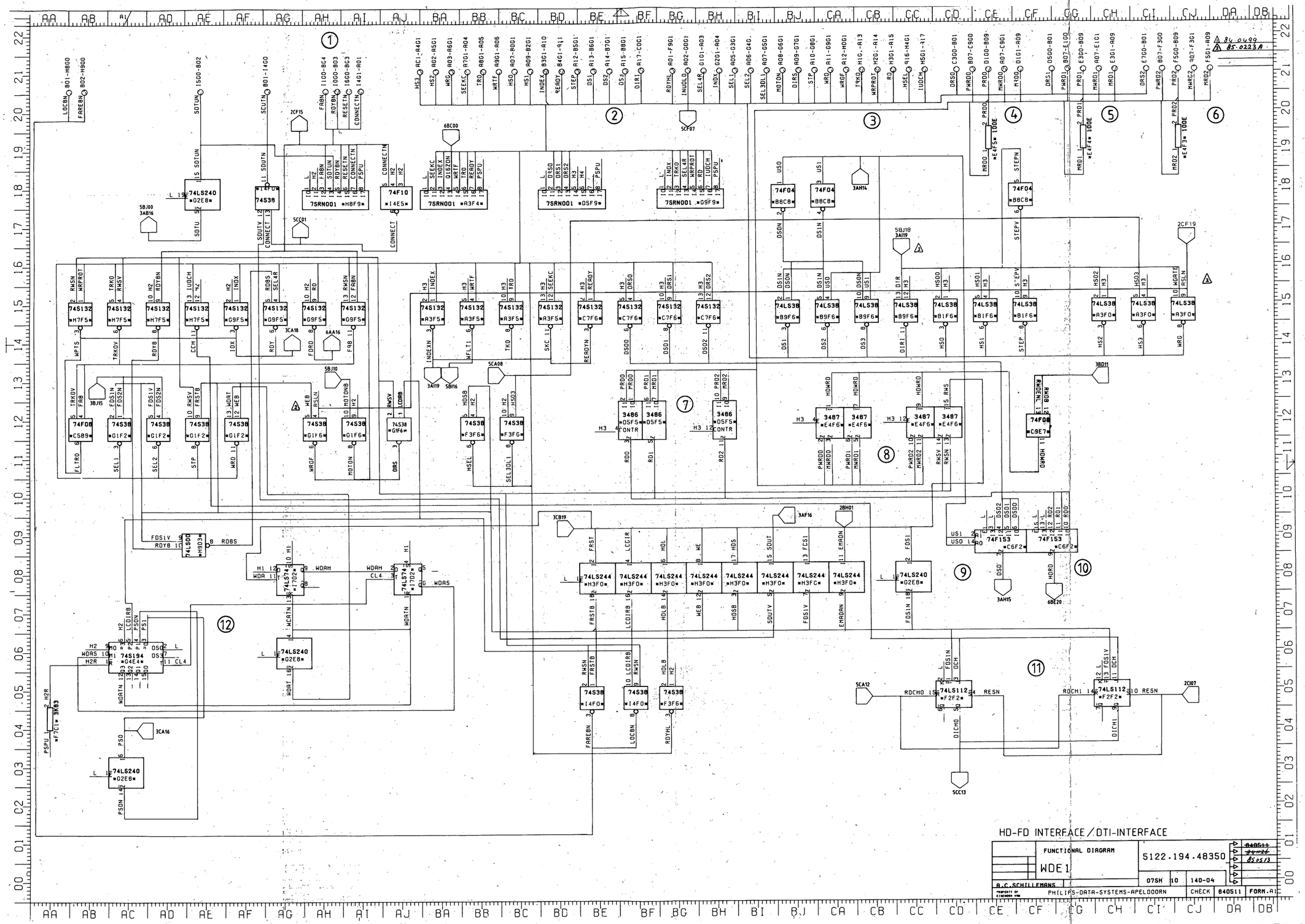


Figure 4.4 HD-FD INTERFACE/ DTI INTERFACE

(1) STATUS REG.

(2) READY 8085

(3) FPLA's

(4) I/O MEM MAP SIGNALS

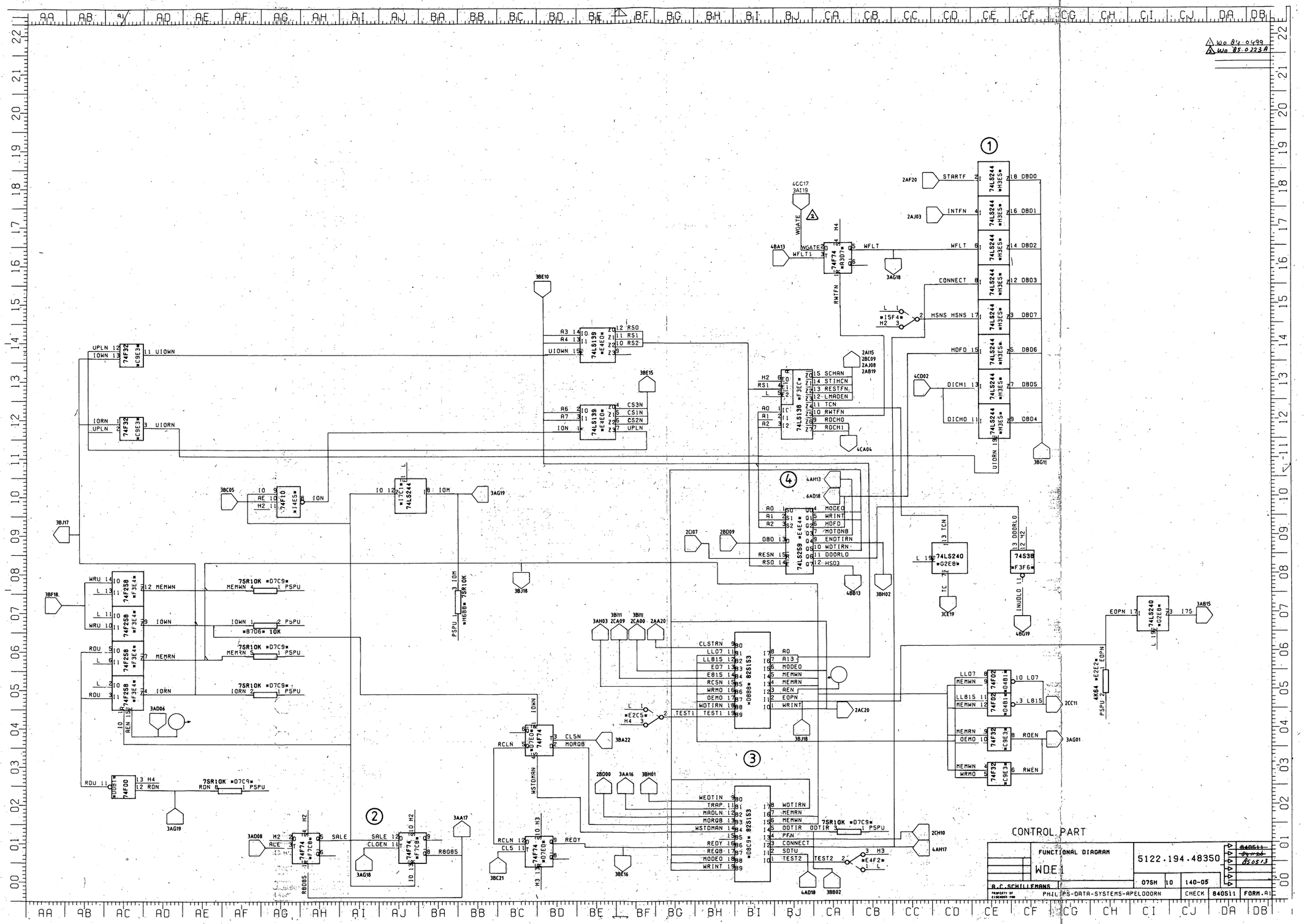
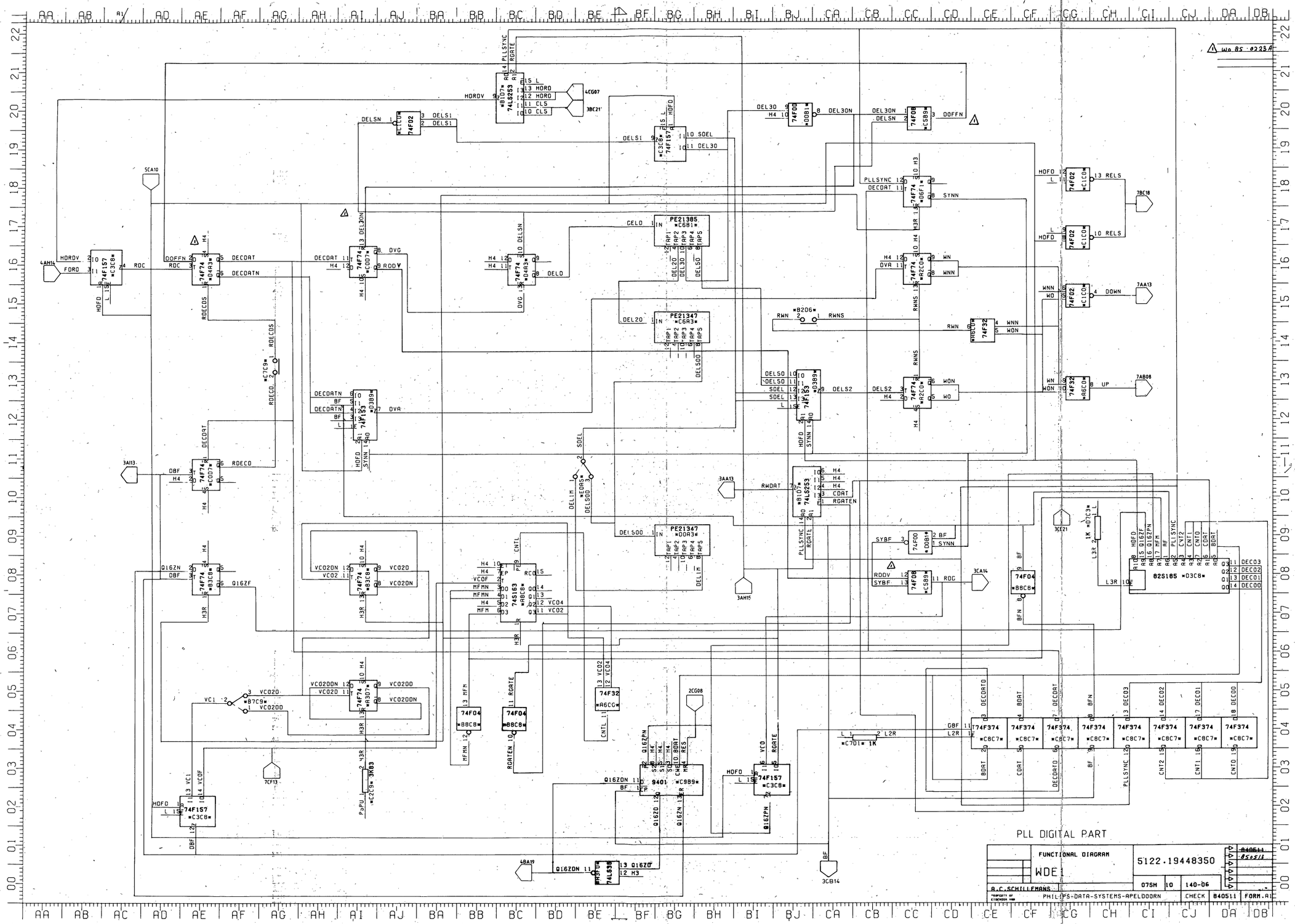


Figure 4.5 CONTROL PART

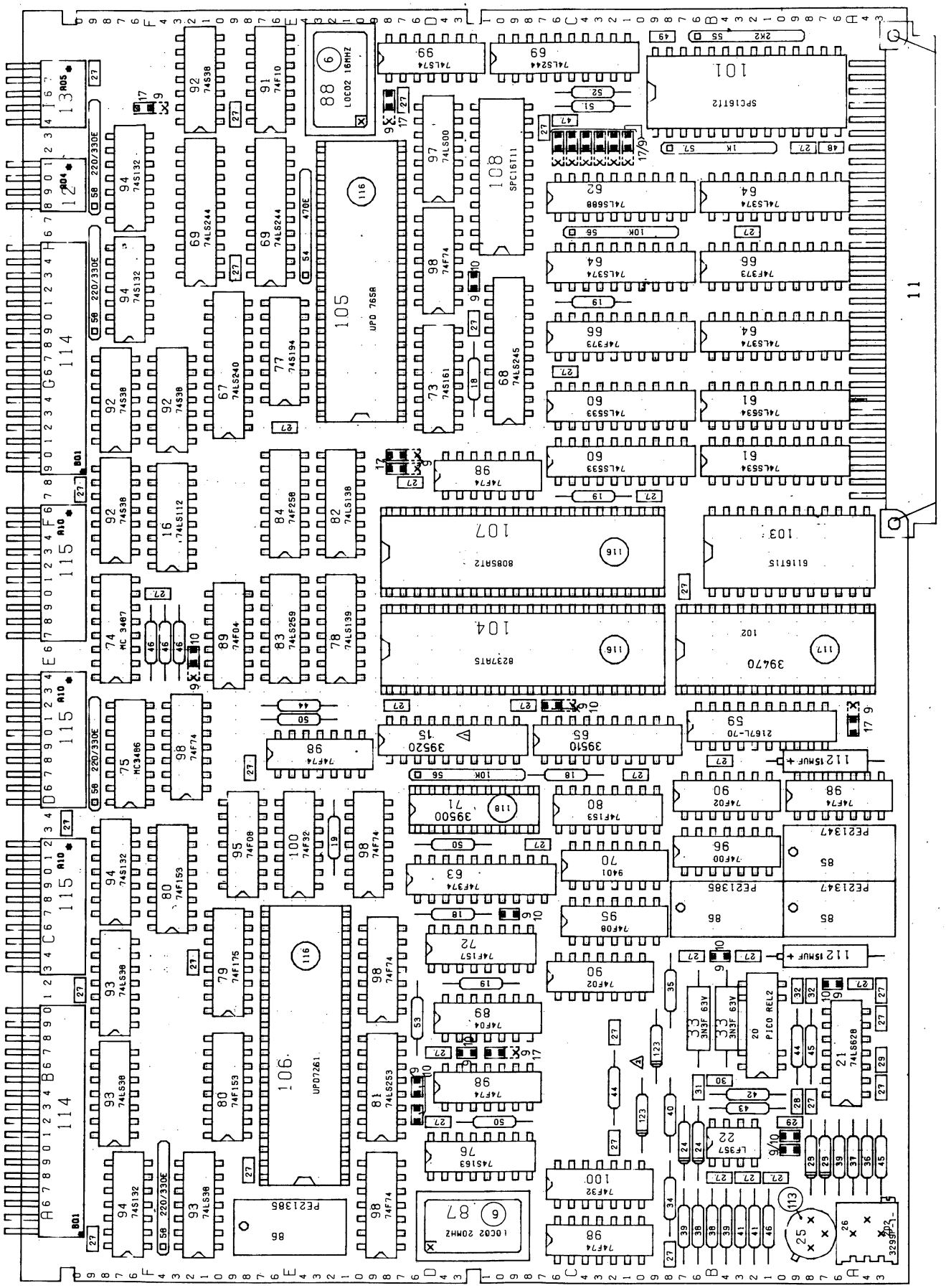

PLL DIGITAL PART
FUNCTIONAL DIAGRAM
WDE1
5122.19448350
A.C.SCHILLEMANS
PHILIPS-DATA-SYSTEMS-APELDOORN
74LS253 *B107*
74F157 *C3C8*
74F74 *D4R3*
74F74 *C0D7*
74F74 *B3C8*
74F74 *A307*
74F74 *A8C8*
74F74 *A2C0*
74F74 *B6F1*
74F74 *C5B9*
74F00 *D0B1*
74F08 *C5B9*
74F04 *B8C8*
74F32 *A6C0*
74F153 *D389*
74F374 *C8C7*
74S163 *A8C8*
82S185 *D3C8*
PE21385 *C6B1*
PE21347 *C6R3*
PE21347 *D0R3*
9401 *C9B9*
74LS38 *A9F0*
74F02 *C1C0*
74F32 *A6C0*
74F04 *B8C8*
74F00 *D0B1*
74F08 *C5B9*
74F04 *C8C8*
74F153 *D389*
74F374 *A2C0*
74F374 *B6F1*
74F374 *C8C7*
82S185 *D3C8*
74F157 *C3C8*
74LS253 *B107*
74F74 *A307*
74F74 *B3C8*
74F74 *C0D7*
74F74 *D4R3*
74F74 *A2C0*
74F74 *B6F1*
74F74 *C5B9*
74F74 *A8C8*
74F74 *C8C7*
74F74 *D0B1*
74F74 *C1C0*
74F74 *A6C0*
74F74 *B8C8*
74F74 *A307

(1) RELAIS SELECTION PLL FOR HD/FD

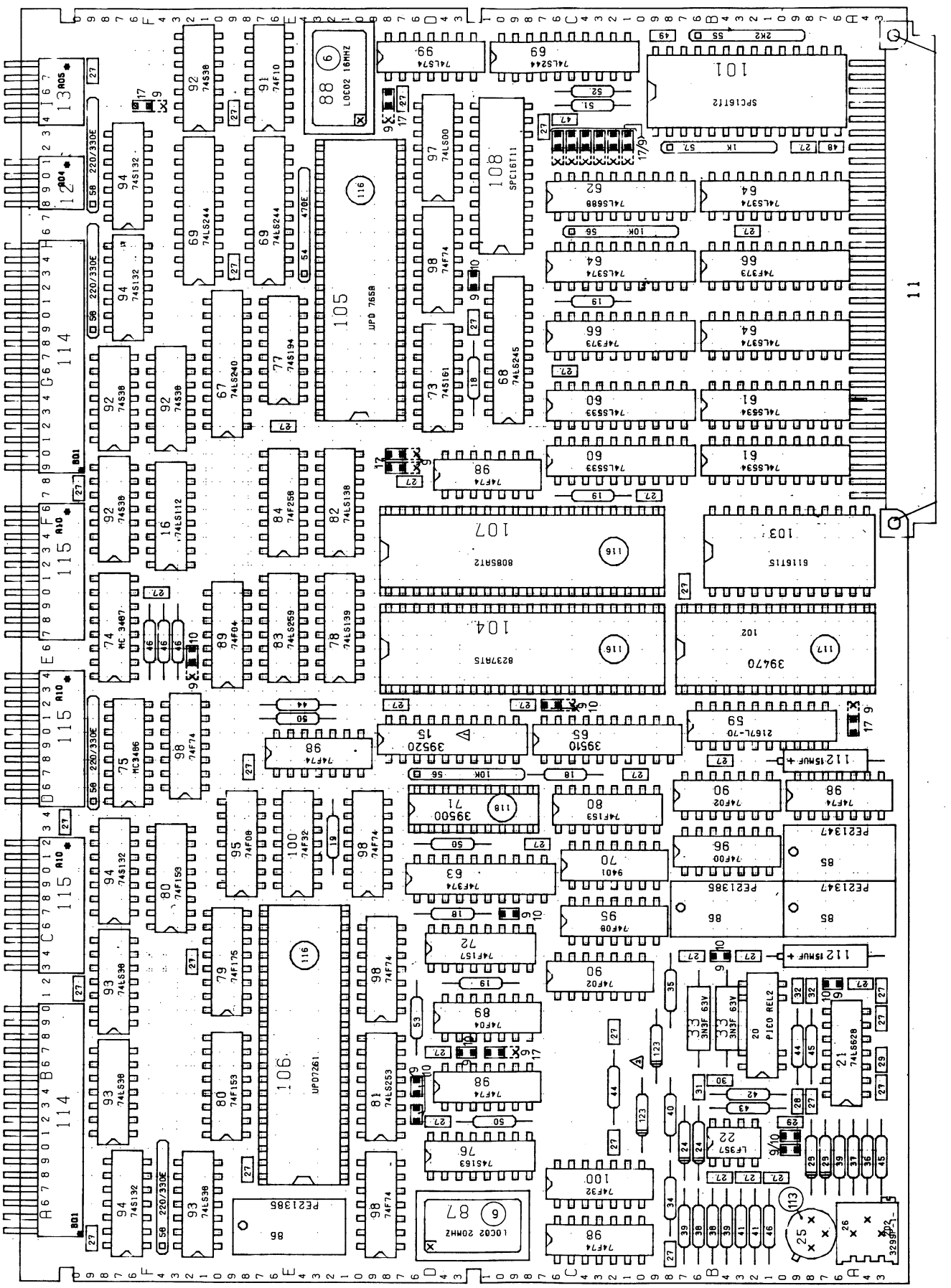
(2) VOLTAGE CONTROLLED OSCILL.

(3) AMPLIFIER

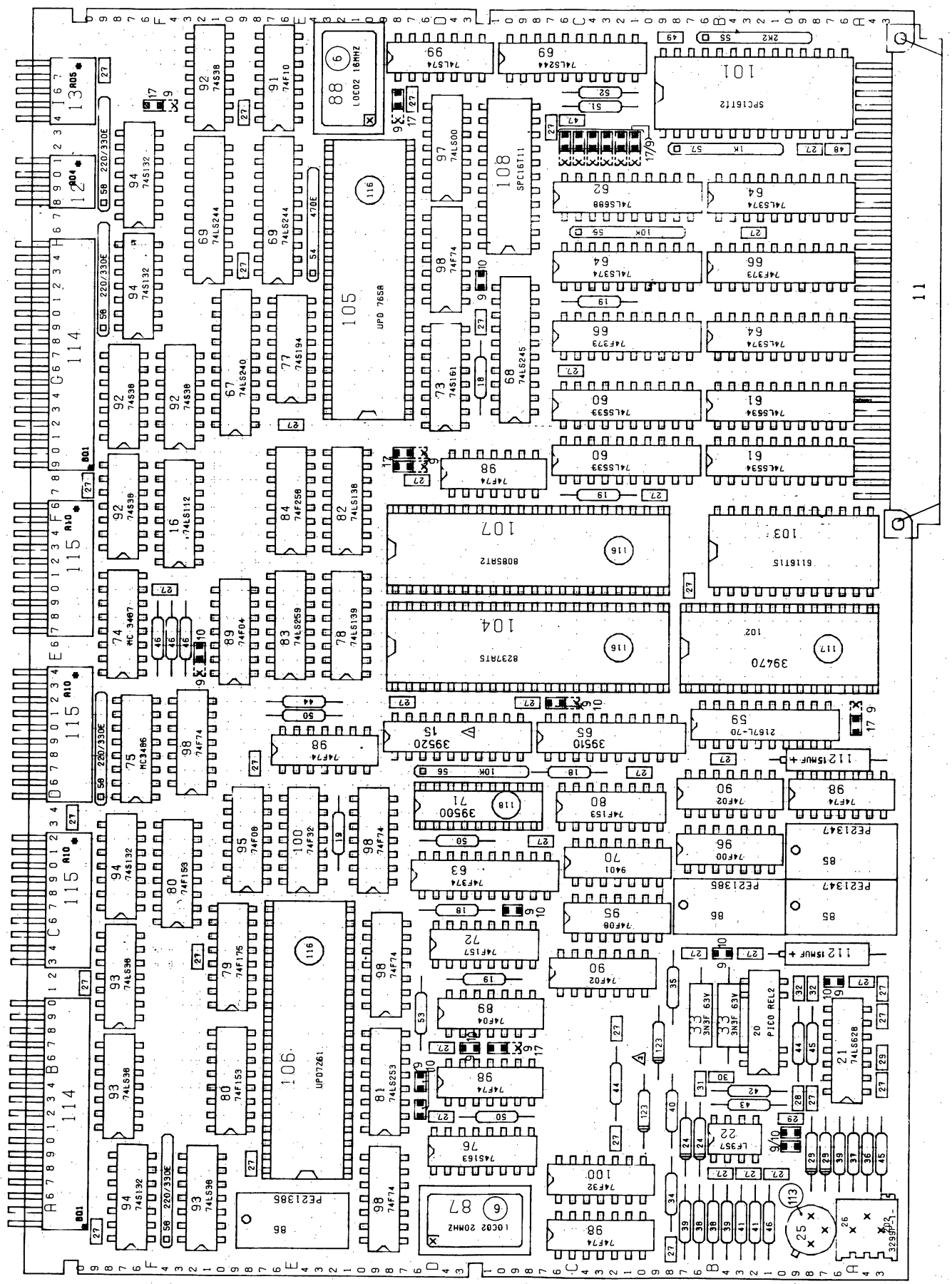
Figure 4.7 PLL DIGITAL PART



Pos.	Code Number	Description
A	5122 194 48350	PCB WDE1 Compl. (Rev. level 7)
1B	5122 194 48360	Print WDE1 (level 1)
2B	5122 110 85590	Text Holder Standard 6E
5B	5122 110 85610	Ejection-Safety Device
9B	5122 000 17170	Male Header 1-RA-1-32
10B	5122 000 16700	Jumper 1-2P-RD
11B	5122 000 11630	Con. Male 3R96ABC
12B	5122 000 13240	M.H.1-RA-2R08A04
13B	5122 000 13260	M.H.1-RA-2R10A05
15B	5122 194 63240	FPLA-2
16B	5122 000 09410	2 x JK-FF 74LS112
17B	5122 000 13890	Jumper 1-2P-GR
18B	2322 151 51002	MTL Film RST MR25 1% 1K
19B	2322 151 53832	MTL Film RST MR25 1% 3K83
20B	5122 000 14520	Reed Relais PMRE2A005B
21B	5122 000 14490	VCO
22B	5122 000 14700	JFET OP-AMP LF357
23B	5122 000 14540	Schottky Diode BAT85
24B	5122 000 14530	Diode BA221
25B	5122 000 11240	+5 Volt. Reg. uA78M05
26B	5122 000 14510	CERM POTM PRES 3299P 10%
27B	5122 000 11820	CER CAP -20+80% 100nF
28B	2222 631 10399	CER CAP 1B 100V 2% 39pF
29B	2222 631 10159	CER CAP 1B 100V 2% 15pF
30B	2222 631 10479	CER CAP 1B 100V 2% 47pF
31B	2222 631 70331	CER CAP 1 100V 2% 330pF
32B	2222 631 70471	CER CAP 1 100V 2% 470pF
33B	2222 428 83302	Micro POCO 63V 1% 3.3nF
34B	2322 151 52611	MTL Film RST MR25 1% 261E
35B	2322 151 51471	MTL Film RST MR25 1% 147E
36B	2322 151 52151	MTL Film RST MR25 1% 215E
37B	2322 151 58259	MTL Film RST MR25 1% 82E5
38B	2322 151 55628	MTL Film RST MR25 1% 5E62
39B	2322 151 51211	MTL Film RST MR25 1% 121E
40B	2322 151 51963	MTL Film RST MR25 1% 19K6
41B	2322 151 51213	MTL Film RST MR25 1% 12K1
42B	2322 151 56812	MTL Film RST MR25 1% 6K81
43B	2322 151 56342	MTL Film RST MR25 1% 6K34
44B	2322 151 54642	MTL Film RST MR25 1% 4K64
45B	2322 151 55621	MTL Film RST MR25 1% 562E
46B	2322 151 51001	MTL Film RST MR25 1% 100E
47B	2222 630 01332	CER CAP 2 100V 10% 3.3nF
48B	2222 631 52151	CER CAP 1B 100V 2% 150pF
49B	2222 631 46121	CER CAP 1B 100V 2% 120pF
50B	2322 151 54641	MTL Film RST MR25 1% 464E



Pos.	Code Number	Description
51B	2322 151 52152	MTL Film RST MR25 1% 2K15
52B	2322 151 53161	MTL Film RST MR25 1% 316E
53B	2322 151 51003	MTL Film RST MR25 1% 10K
54B	5122 000 11480	SIL 0.2W 7x470E
55B	5122 000 11800	SIL 0.2W 7x2K2
56B	5122 000 11500	SIL 0.2W 7x10K
57B	5122 000 11490	SIL 0.2W 7x1K
58B	5122 000 11890	SIL 0.2W 220E/330E
59B	5122 000 14400	IC SRAM,16K*1 2167L-70
60B	5122 000 14120	IC Inv.Oct.Latch 74LS533
61B	5122 000 14130	IC Inv.Oct.D-Reg. 74LS534
62B	5122 000 12750	IC 8B. Comperator 74LS688
63B	5122 000 13080	IC 8 x D-FF 74F374
64B	5122 000 10750	IC 8 x D-FF 74LS374
65B	5122 194 56470	IC FPLA-1
66B	5122 000 13070	IC 8 x D-Latch 74F373
67B	5122 000 10600	IC 8*BUF Inv,3ST. 74LS240
68B	5122 000 14170	IC Oct.Bus Transc 74LS245
69B	5122 000 11190	IC 8 x BUFF.3-ST 74LS244
70B	5122 000 11260	IC CRC Gen./Check 9401
71B	5122 194 56450	IC PLL PROM
72B	5122 000 13040	IC 4 x 2-MUX 74F157
73B	5122 000 10880	IC 4-Bit BIN.CNT 74S161
74B	5122 000 11590	IC 4 x RS422 DR. 3487
75B	5122 000 11780	IC 4x RS422/3 REC 3486
76B	5122 000 10890	IC 4-Bit BIN.CNT 74S163
77B	5122 000 09590	IC 4-Bit SH.Reg. 74S194
78B	5122 000 09970	IC 2 x 2 to 4 DEC 74LS139
79B	5122 000 13530	IC 4 x D-FF 74F175
80B	5122 000 13030	IC 2 x 4-MUX 74F153
81B	5122 000 09680	IC 2 x 4-MUX 3ST 74LS253
82B	5122 000 09170	IC 1 x 3 to 8 DEC 74LS138
83B	5122 000 10640	IC 8*Addres.Latch 74LS259
84B	5122 000 13750	IC 4*2 MX INV 3ST 74F258
85B	5122 000 14470	IC DEL.LIN.5*100 21347
86B	5122 000 14480	IC DEL.LIN.5*10N 21385
87B	5122 000 14460	OSC.20.0000MHz LOCO20.0
88B	5122 000 11320	OSC.16.0000MHz LOCO16.0
89B	5122 000 13570	IC 6 x Inverter 74F04
90B	5122 000 13470	IC 4 x 2 INP NOR 74F02
91B	5122 000 13600	IC 3 * 3 INP NAND 74F10
92B	5122 000 09960	IC 4*2-INP NA O.C. 74S38
93B	5122 000 09670	IX 4 x 2-INP NAND 74LS38
94B	5122 000 09480	IC 4*2INP SCHM-TR 74S132
95B	5122 000 12990	IC 4 x 2-INP and 74F08



Pos.	Code Number	Description
96B	5122 000 13460	IC 4 x 2-INP NAND 74F00
97B	5122 000 09120	IC 4 x 2 INP NAND 74LS00
98B	5122 000 13010	IC 2 x D-FF 74F74
99B	5122 000 09150	IC 2 x D-FF 74LS74
100B	5122 000 13000	IC 4 x 2-INP.OR 74F32
101B	5122 000 13161	IC BUS-LSI SPC16-12
102B	5122 000 62070	IC MPR 5 1/4 DCU
103B	5122 000 13130	IC SRAM,2K*8 6116-15
104B	5122 000 13660	IC Prog.DMA.Contr.8237A-5
105B	5122 000 14500	IC Floppy Disk CTR 765A
106B	5122 000 14410	IC Hard Disk CTRL 7261
107B	5122 000 13640	IC 8 Bit U-PROC 8085A-2
108B	5122 000 13150	IC Int. Handler SPC16-11
112B	2022 001 00159	Tantalum Cap 20V
113B	2412 490 00338	Mount Pad To-5/18
114B	8222 069 11803	Con. M.H.1-RA-2R34B01
115B	8222 069 11804	Con. M.H.1-RA-2R20A10
116B	5122 000 11440	IC Dil Socket Low 40P-6E
117B	5122 000 11430	IC Dil Socket Low 28P-6E
118B	5122 000 11400	IC Dil Socket Low 18P-3E
119B	5122 000 17160	Male Header 1-RA-2-64
120B	5122 111 05110	Cover for D.E. Card SH MAX9
121B	5122 111 05410	Foam Plate 155 x 226 Antistatic
123B	5122 000 17520	Shottky Diode 5082-2835

FACTORY CODE NUMBER	SERVICE CODE NUMBER	DESCRIPTION
2022 001 00159	5322 124 10017	CAP 15UF 20V 20%
2222 428 83302	5322 121 54049	CAP 3.3NF 63V 2%
2222 630 01332	4822 122 30099	CAP 3.3NF 100V 10%
2222 631 10159	4822 122 31058	CAP 15PF
2222 631 10399	4822 122 31069	CAP 39PF 100V 2%
2222 631 10479	4822 122 31072	CAP 47PF 500V 2%
2222 631 46121	5322 122 34156	CAP 120PF 100V %
2222 631 52151	4822 122 31285	CAP 150PF 100V
2222 631 70331	5322 122 34148	CAP 330PF 100V
2222 631 70471	5322 122 34159	CAP 470PF 100V
2322 151 51001	5322 116 55549	RES 100E 1% 0.4W
2322 151 51002	4822 116 51235	RES 1K 1% 0,4W
2322 151 51003	4822 116 51253	RES 10K 1% 0.4W
2322 151 51211	5322 116 54426	RES 121E 1% 0.4W
2322 151 51213	5322 116 50572	RES 12K1 1% 0.4W
2322 151 51471	5322 116 50766	RES 147E 1% 0.25W
2322 151 51963	5322 116 54641	RES 19K6 1% 0.25W
2322 151 52151	5322 116 55274	RES 215E 1% 0.25W
2322 151 52152	5322 116 50767	RES 2K15 1% 0.25W
2322 151 52611	5322 116 54502	RES 216E 1% 0.25W
2322 151 53161	5322 116 54511	RES 316E 1% 0.25W
2322 151 53832	5322 116 54589	RES 3K83 1% 0.4W
2322 151 54641	5322 116 50536	RES 464E 1% 0.4W
2322 151 54642	5322 116 50484	RES 4K64 1% 0.25W
2322 151 55621	4822 116 51231	RES 562E 1% 0.4W
2322 151 55628	5322 116 54128	RES 5E6 1% 0.4W
2322 151 56342	5322 116 54602	RES 6K34 1% 0.4W
2322 151 56812	4822 116 51252	RES 6K81 1% 0,4W
2322 151 58259	4822 116 52814	RES 82E5 1% 0.4W
5122 000 09120	5322 209 84823	IC N74LS00A
5122 000 09150	4822 209 80782	IC 74LS74
5122 000 09170	5322 209 85647	IC N74LS138B
5122 000 09410	5322 209 84971	IC 74LS112
5122 000 09480	5322 209 85267	IC 74S132
5122 000 09590	5322 209 86061	IC N74S194F
5122 000 09670	5322 209 85605	IC N74LS38A
5122 000 09680	5322 209 85667	IC SN74LS253N
5122 000 09960	5322 209 85677	IC N74S38A
5122 000 09970	5322 209 85839	IC N74LS139N
5122 000 10600	5322 209 85862	IC SN74LS240N
5122 000 10640	5322 209 86007	IC SN74LS259N
5122 000 10750	5322 209 85869	IC SN74LS374AN
5122 000 10880	5322 209 85698	IC SN74S161N
5122 000 10890	5322 209 85915	IC SN74LS161AN
5122 000 11190	5322 209 86017	IC N74LS244N
5122 000 11240	5322 209 84841	IC 78M05C4
5122 000 11260	5322 209 85514	IC 9401DC
5122 000 11320	5322 242 74379	OSCILL 16MHZ LOCO
5122 000 11400	5322 255 44233	SOCKET 18POL. (DIL)
5122 000 11430	5322 255 44234	SOCKET 28POL. (DIL)
5122 000 11440	5322 255 44235	SOCKET 40POL. (DIL)
5122 000 11480	5322 111 94226	RES 7SR470
5122 000 11490	5322 111 94227	RES 7SR 1K
5122 000 11500	5322 111 94228	RES 7SR10K
5122 000 11590	5322 209 86196	IC MC3487P
5122 000 11630	5322 265 64104	CONN
5122 000 11780	5322 209 14733	IC MC3486P
5122 000 11820	5322 122 34153	CAP 100NF 50V %
5122 000 11890	5322 111 94276	RES 7SR230
5122 000 12750	5322 209 80976	IC 74LS688

FACTORY CODE NUMBER	SERVICE CODE NUMBER	DESCRIPTION
5122 000 12990	5322 209 81574	IC 74F08
5122 000 13000	4822 209 82133	IC 74F32
5122 000 13010	5322 209 81474	IC 74F74PC
5122 000 13030	5322 209 81575	IC 74F153
5122 000 13040	5322 209 81531	IC 74F157
5122 000 13070	5322 209 81533	IC 74F373
5122 000 13080	5322 209 81909	IC 74F374
5122 000 13150	5322 209 86209	ROM SPC16-11 (IHC)
5122 000 13160	5322 209 86197	ROM SPC16-12(BUS-LSI
5122 000 13260	5322 265 40188	CONN 75176 9P
5122 000 13460	5322 209 81534	IC 74F00
5122 000 13470	5322 209 81535	IC 74F02
5122 000 13530	5322 209 81542	IC 74F175
5122 000 13570	5322 209 81577	IC 74F04
5122 000 13600	5322 209 81681	IC 74F10
5122 000 13640	5322 209 81916	IC 8085A-2
5122 000 13750	5322 209 81769	IC 74F258
5122 000 13890	5322 263 60062	FEMALE TEST COMA
5122 000 14120	5322 209 82152	IC 74LS533
5122 000 14130	5322 209 82037	IC SN74LS534N
5122 000 14170	5322 209 86225	IC 74LS245
5122 000 14400	5322 209 82481	IC 2167L-70
5122 000 14500	5322 209 81743	FLOPPY DISKCTR 765A
5122 000 14530	4822 130 30831	DIODE BA221
5122 000 14540	4822 130 31983	DIODE BAT85
5122 194 48350	5322 216 21586	PCB WDE

service information | FIELD CHANGE | Data Systems

system series: P800, P4000, P6000, P9000
model: P829, P4200, P4202/P4402, P4502/P4802, P6923, P9200/P9300
main assy: PCB WDE **nr.** P829-C-007, P4500-222, P6923-016, P9000-028
units affected: All
est.inst.time: 45 min.
date: 851007 **revised:**

title: WDE problems

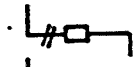
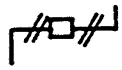
note: Previous SI P4200-023

this change is: Mandatory

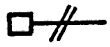
1. CONDITION : - Excessive recoverable errors on track zero of the flexible disk.
   - False "Write fault" indication from the Seagate 10M fixed disks.
   - When switching power on, data sets can be overwritten if the fixed and/or flexible disks are located in an extension cabinet (P3437, P3438, P9101).

2. CORRECTION : Modify the PCB WDE.

3. REMOVE : IC 74F08 at location C5B9. This IC is removed only to facilitate the modification it is then replaced.
   On componentside, cut the following printed connections:

   C1C6 
   C8C3 
   A8F3 
   G4F6 

   On soldering side:

   C8C4 
   A4D7 
   A5F3 

4. ADD : IC 74F08 at location C5B9.

   On soldering side, make the following connections:

D6C4 - D0B7	J0C3 - G4F6
C1E0 - C5C5	G4F6 - A8F3
C8C3 - C5E0	C9C5 - D0B6
C8C4 - D0B5	A7F5 - A5F3
A8E5 - A4D7	G6F9 - G4F3

5. ADJUSTMENTS : None.

service information

Data Systems

revised: nr. P829-C-007
P4500-222
P6923-016
P9000-028

6. PARTS :

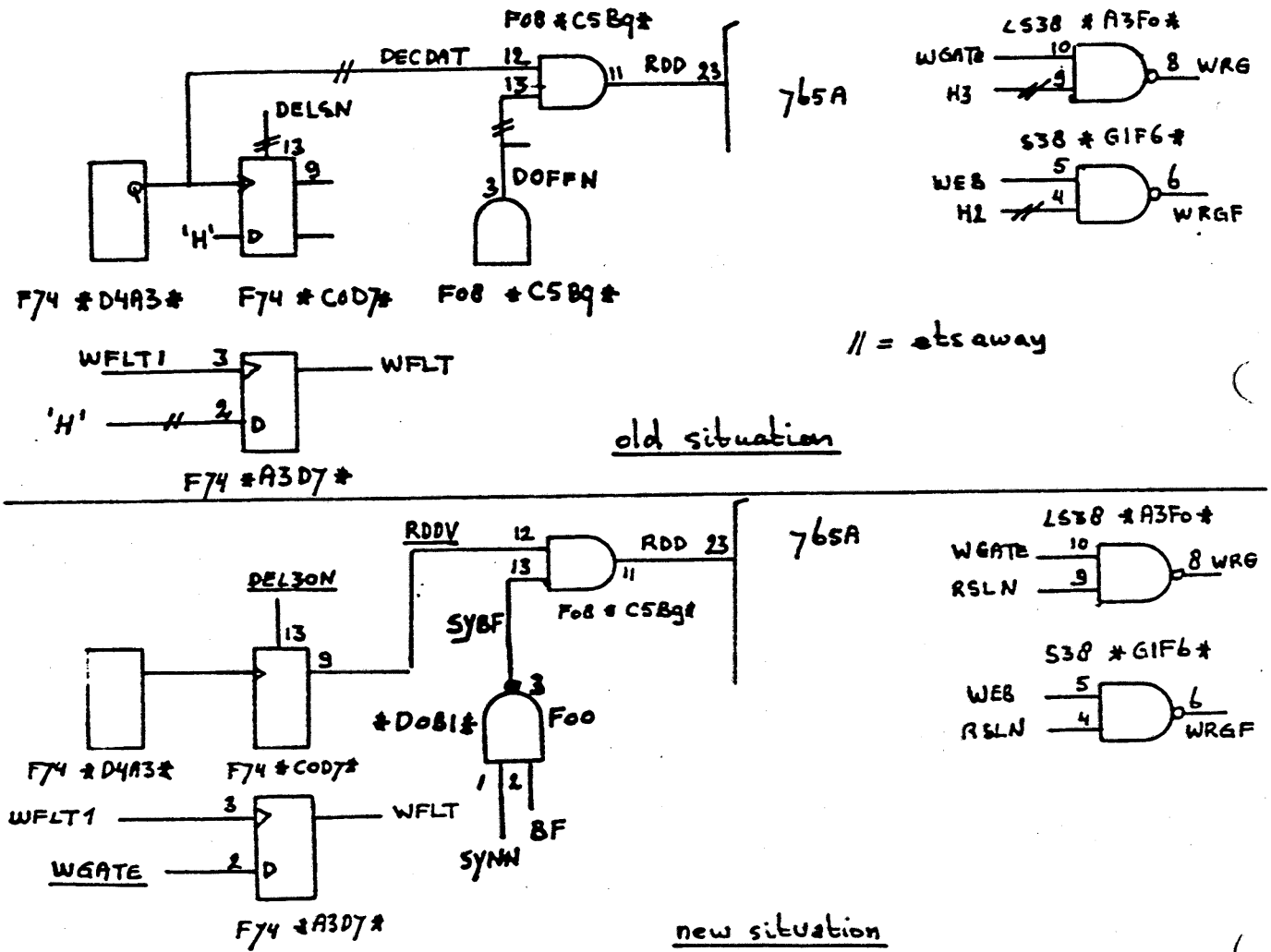
Description	Service 12NC
IC 74F08	5322 209 81574

7. STATUS CHANGE : Change the 12NC of PCB WDE from 5122 194 48353 into 5122 194 48354 and cross off mod 03.
The service 12NC: 5322 216 21586 is not changed.

8. TEST FACILITIES AFFECTED : None.

9. DOCUMENTS AFFECTED : Schematics 5122 194 48350 sheet 140 pages 4, 5 and 6 (see drawing).

10. REMARKS : Previous SIs for the PCB WDE had only P4200 numbers. Now, the PCB WDE is also used in P4502/P4802 Slimline models, P800, P6000 and P9000 so, the SIs will have P800, P4500, P6000 and P9000 numbers.



service information | FIELD CHANGE | Data Systems

system series: P800, P4000, P6000, P9000
model: P829, P4200, P4202/P4402, P4502/P4802, P6923, P9200/P9300
main assy: PCB WDE **nr.** P829-C-008, P4500-223, P6923-017, P9000-029
units affected: All
est.inst.time:
date: 851007 **revised:**

title: WDE in P4000 Slimline.

note: Previous SI P829-C-007/P4500-222/P6923-017/P9000-029
this change is: SEE REMARKS

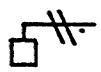
1. CONDITION : The PCB WDE cannot be used in P4000 Slimline. The circuit for determining the CU number is not compatible with the combination of UPL-2 Bus and P4000 HSI.

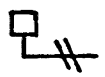
2. CORRECTION : Modify the PCB WDE so it can be used in P4000 Slimline, P4000 present line and P9000.

3. REMOVE : On soldering side cut the following printed connections:

G4C5 

G2A4 

G1A4 

G0A4 

On component side:

I0B6 

4. ADD : None.

5. ADJUSTMENTS : None.

6. PARTS : None.

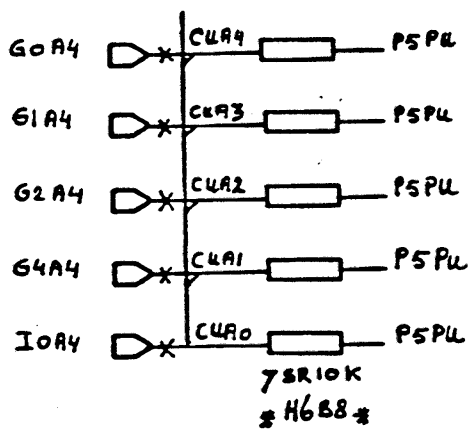
7. STATUS CHANGE : Change the 12NC of PCB WDE from 5122 194 48354 into 5122 194 48355 and cross off mod 04.
The service 12NC: 5322 216 21586 is not changed.

8. TEST FACILITIES AFFECTED : None.

9. DOCUMENTS AFFECTED : Schematics 5122 194 48350 sheet 140 page 2. (see drawing).

10. REMARKS : With this change, the automatic slot recognition is disabled on the WDE so, the straps must always be set for the proper CU number when using the WDE in P4000 present line, P4000 Slimline, P9000, P800 or P6000.
This change is mandatory for a WDE used in P4000 Slimline and Retrofit on failure for a WDE used in P4000 present line, P9000, P6000 and P800.

Functional diagram SH140-2



service information

| TECHNICAL TIP |

Data Systems

system series:	P800	**model:**	P829	**main assy:** PCB WDE	**nr.** P829-C-009
	P4000		P4200		P4500-227
	P6000		P4202/P4402		P6923-018
	P9000		P4502/P4802		P9000-034
			P6923/P6927		
			P9200/P9300		

date: 851122 **revised:**

title: Replacement of BA221 diodes.

note:

The 12NC of the WDE is changed from 5122 194 48355 into 5122 194 48356.
The BA221 diodes at locations B5B9 and B0C0 are replaced by Hewlett Packard diodes 5082-2835.

This is not a functional change, the diodes were changed because the BA221 type had a high rejection rate (± 2%) during production and testing.

On the PCBs in the field the diodes have been tested so the 12NC can be changed from 5122 194 48355 into 5122 194 48356 without changing the diodes.
The Mod. number 04 and service 12NC: 5322 216 21586 are not changed.

Previous SI P829-C-008
P4500-223
P6923-017
P9000-029

Responsibility: Mr. E. Silva.

service information

PHILIPS

| FIELD CHANGE |

system series: P800 P4000 P6000 P9000
model: P829 P4200 P4202/P4402 P4502/P4802 P6923 P9200/P9300
main assy: PCB WDE1 **nr.** P829-C-011 P4700-021 P6925-223 P9000-059
units affected: All
est.inst.time: 2 hours
date: 860522 **revised:** 860827

title: Microprogram release 1 for WDE1 (new PROM 40021).

note: Previous SI P829-C-009/P4500-227/P6923-018/P9000-034
this change is: Retrofit on failure

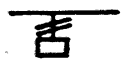
1. CONDITION : Microprogram Rel. 1 was planned to be introduced with release of WDI.
For WDE it is introduced as well, because of hard disk performance improvement by seek overlap. In practice this improvement is only noticeable when a data management system uses more than one hard disk drive.

2. CORRECTION : The microprogram size is doubled to 16kB (before = 8kB), so an additional addressline is needed (= A14). This addressline is also led to FPLA-1 and FPLA-2 for RAM selection .

3. REMOVE : On component side (see page 2)

- EPROM, type 2764-3, location E3A4.
- IC socket where EPROM is mounted on.
- FPLA-2, type 82S153, location D8C9.
- Strap test 2, location E4F2 (see page 2).

Cut the following connections:

- P5PU  E9B5 component side
- (A13)  E9A9 soldering side
- (A13)  D8A9 soldering side

4. ADD : Remount IC socket
EPROM 27128-3 at location E3A4
FPLA-2 82S153 at location D8C9

On the soldering side make the following connections:

- F1A9 - E9B5 (A13)
- F6C5 - E9A9 (A14)
- D8C1 - F6C5 (A14)
- D8D8 - D8C1 (A14)

5. ADJUSTMENTS : None.

Responsibility: Mr. B. Berends.

CO 86.0211

6. PARTS :

Description	12NC
EPROM	5122 194 40021
FPLA-2	5122 194 39522

PROMs can be orderd from:

Philips TDS
Dept. Customer Service Material Management
Att. Mr. A. Versloot
Apeldoorn

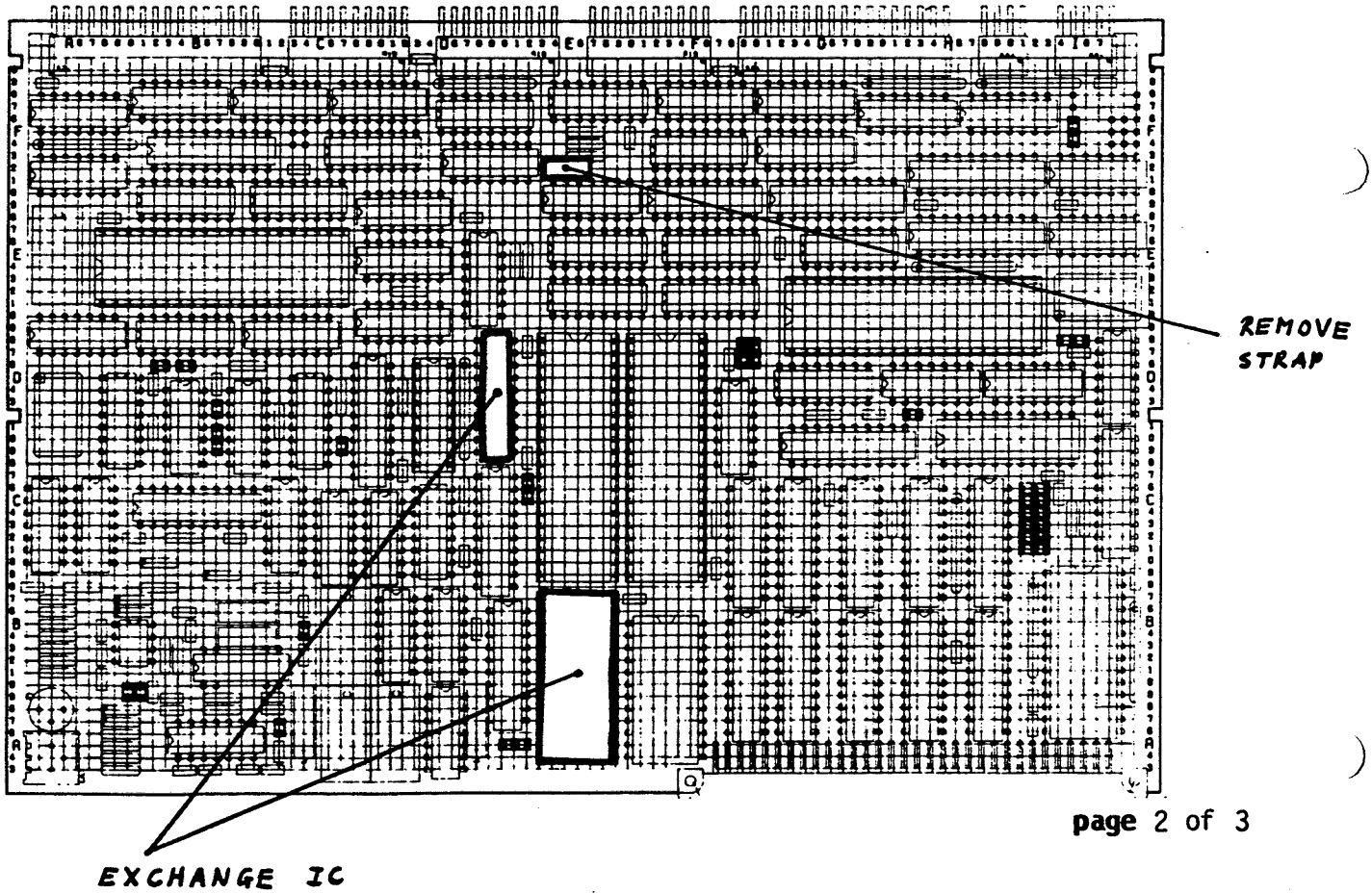
7. STATUS CHANGE : This is Mod. 5 of the PCB WDE1.
The 12NC changes from 5122 194 48356 into 5122 194 48357.
Service 12NC: 5322 216 21586 not changed.

8. TEST FACILITIES AFFECTED : None.

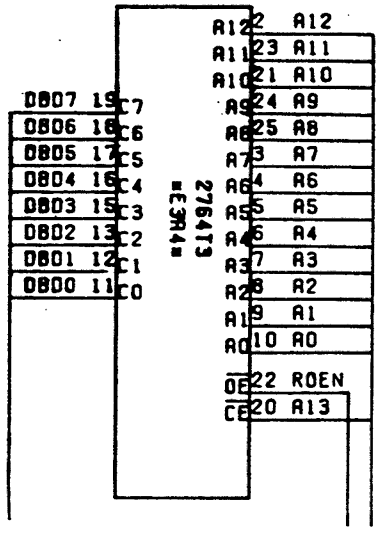
9. DOCUMENTS AFFECTED : Schematics 5122 194 48350 sheet 140 pages 3 and 5 (see page 3).

10. REMARKS : From this mod. level on additional improvement on IPL and overlay loading can be achieved by using a utility. "Program Load Improvement".

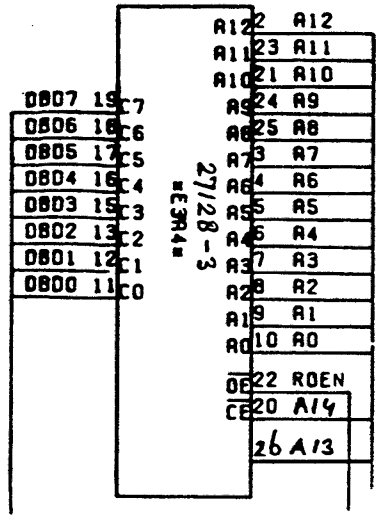
The utility will be part of the SSS tool information system and will be announced by SSS.



revised: nr. P829-C-011
P4700-021
P6925-223
P9000-059

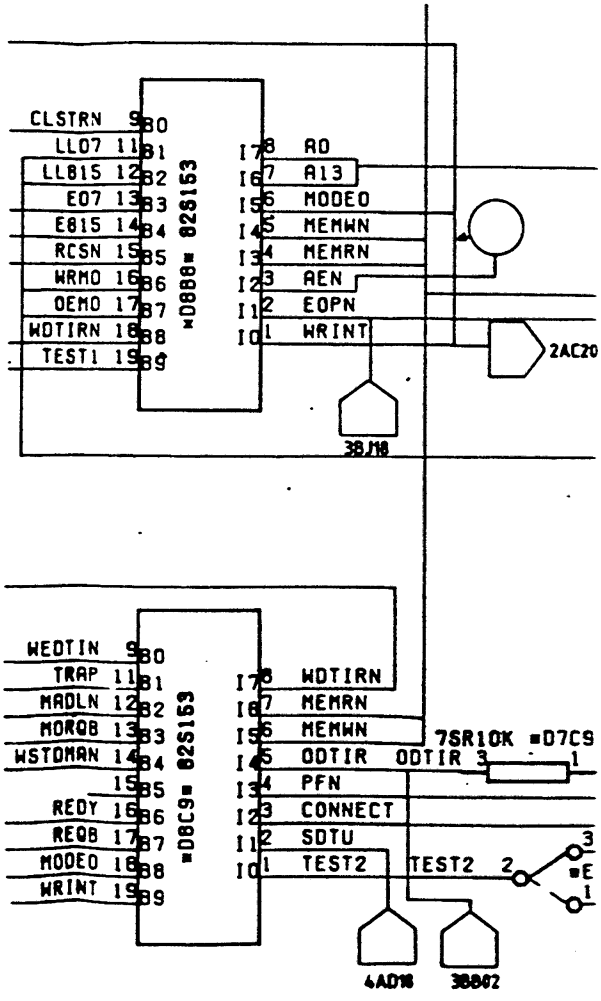


Old

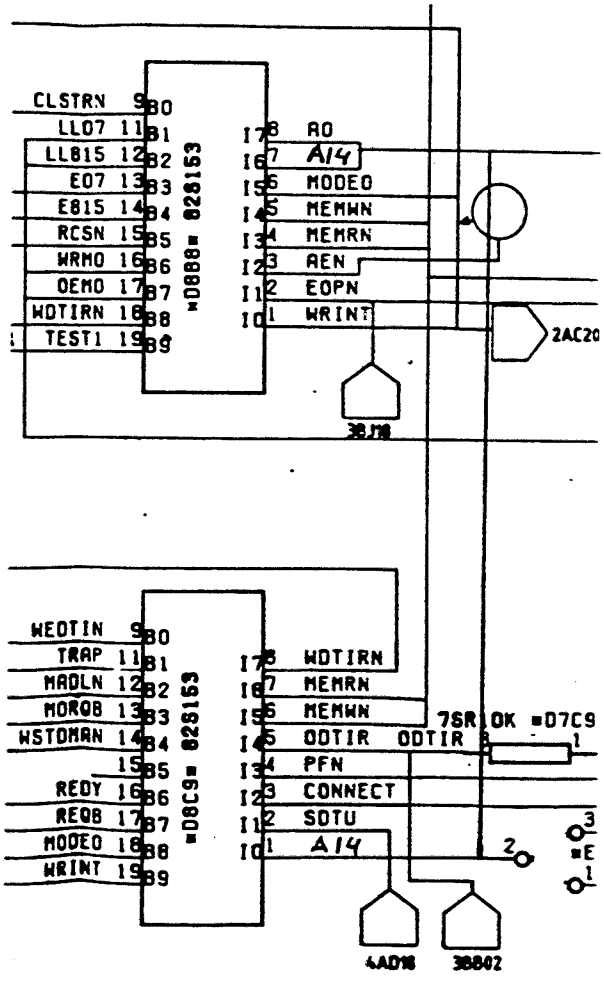


New

On schematics 5122 194 48350 sheet 140-3.



Old



New

On schematics 5122 194 48350 sheet 140-5.

service information

FIELD CHANGE

system series: P800, P4000, P6000, P9000
model: P829, P4200, P4202/P4402, P4502/P4802, P6923, P9200/P9300
main assy: PCB WDE1 **nr.** P829-C-014, P4700-035, P6925-232, P9000-072
units affected: All
est.inst.time: 10 min.
date: 860916 **revised:**

title: Microprogram release 2 for WDE1.

note: See status change.
this change is: Retrofit on failure

1. CONDITION : IPL does not work when during READ a Peripheral Attention Interrupt is received from another fixed disk connected to the same WDE.

2. CORRECTION : Exchange of microprogram.

3. REMOVE : EPROM, type 27128-3/40021, location E3A4.
(MPR identification name: 5122 194 62071).

4. ADD : EPROM type 27128-3/40022, location E3A4.
(MPR identification name: 5122 194 62072).

5. ADJUSTMENTS : None.

6. PARTS :

Description	12NC
EPROM	5122 194 40022

7. STATUS CHANGE : Mark Mod. 6 on PCB WDE1.
FActory 12NC's 5122 194 48357 is unfortunately not changed due to a mistake in the factory.
Boards which have the new EPROM Rev. level already, should be marked Mod. 6.
Service 12NC: 5322 216 21586 not changed.

8. TEST FACILITIES AFFECTED : None.

9. DOCUMENTS AFFECTED : Partslist.
Before starting this modification be shure that Mod. 5 was carried out.
(SI P829-C-011/P4700-021/P6925-223/P9000-059).

10. REMARKS : PROMs can be ordered from:

Philips TDS
Dept. Customer Service Material Management
Att. Mr. A. Versloot
Apeldoorn

Responsibility: Mr. B. Berends.

service information | FIELD CHANGE |

system series: P800	**model:** P829	**main assy:** PCB WDE1	**nr.** P829-C-015	
P4000	P4200	P829-142	P4000-35	P4700-036
P6000	P4202/P4402	P6966		P6925-234
P9000	P4502/P4802	P6759-001		P6966-002
units affected:	P6923/P6966	**est.inst.time:** 2 hours		P9000-073
	P9200/P9300			

date: 861010 **revised:**

title: IPL from 8" floppy box with WDE-1 used as control unit.

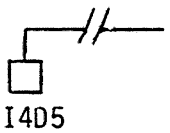
note: **this change is:** Retrofit on condition

1. CONDITION : This modification is only important if an 8" floppy box is connected.
   If the 8" floppy box was adjusted as drive 0 (for IPL), an attach on drive 1 (not present) didn't return a "not operable".

2. CORRECTION : Selection is provided by means of an extra strap.

3. REMOVE : Cut track on soldering side:

   - FDS1N



4. ADD : Strap at location I8F4 (on comp. side)

   Jump by on soldering side:

   I4D6 - I8F5 (SEL8)
   G5F2 - I8F6 (FDS1V)
   G2F2 - I8F4 (FDS1N)

5. ADJUSTMENTS : None.

6. PARTS :

Description	12NC	Amount	Service 12NC
Jumper 1-2P-GR	5122 000 13890	1	5322 263 60062

7. STATUS CHANGE : This is Mod. 7 of the PCB WDE1.
   The 12NC changes from 5122 194 48357 into 5122 194 48358.
   Service 12NC: 5322 216 21586 not changed.

8. TEST FACILITIES AFFECTED : None.

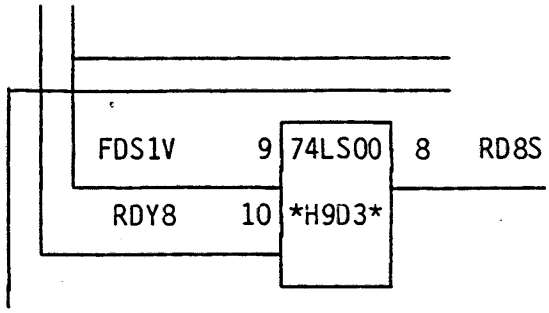
9. DOCUMENTS AFFECTED : None.

10. REMARKS :
    - WDE-1 is not used as 8" floppy control unit in P6000 and P800.
    - Dipswitch adjustment on drive in floppy box:
      Ready 2 switch should always be closed.

Responsibility: Mr. B. Berends.

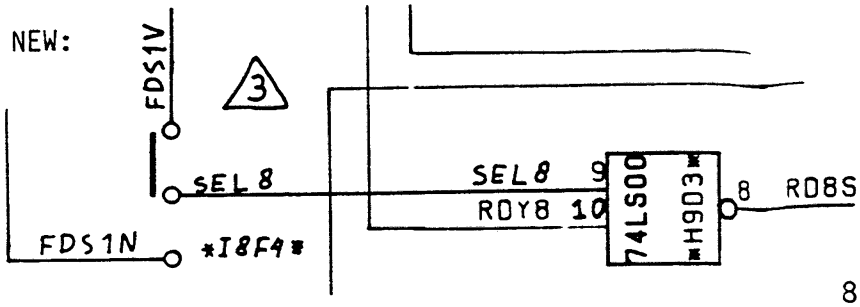
revised: **nr.** P829-C-015
P4700-036
P6925-234
P6966-002
P9000-061

OLD:



New on schematics 5122 194 48350 sheet 140-04:

NEW:

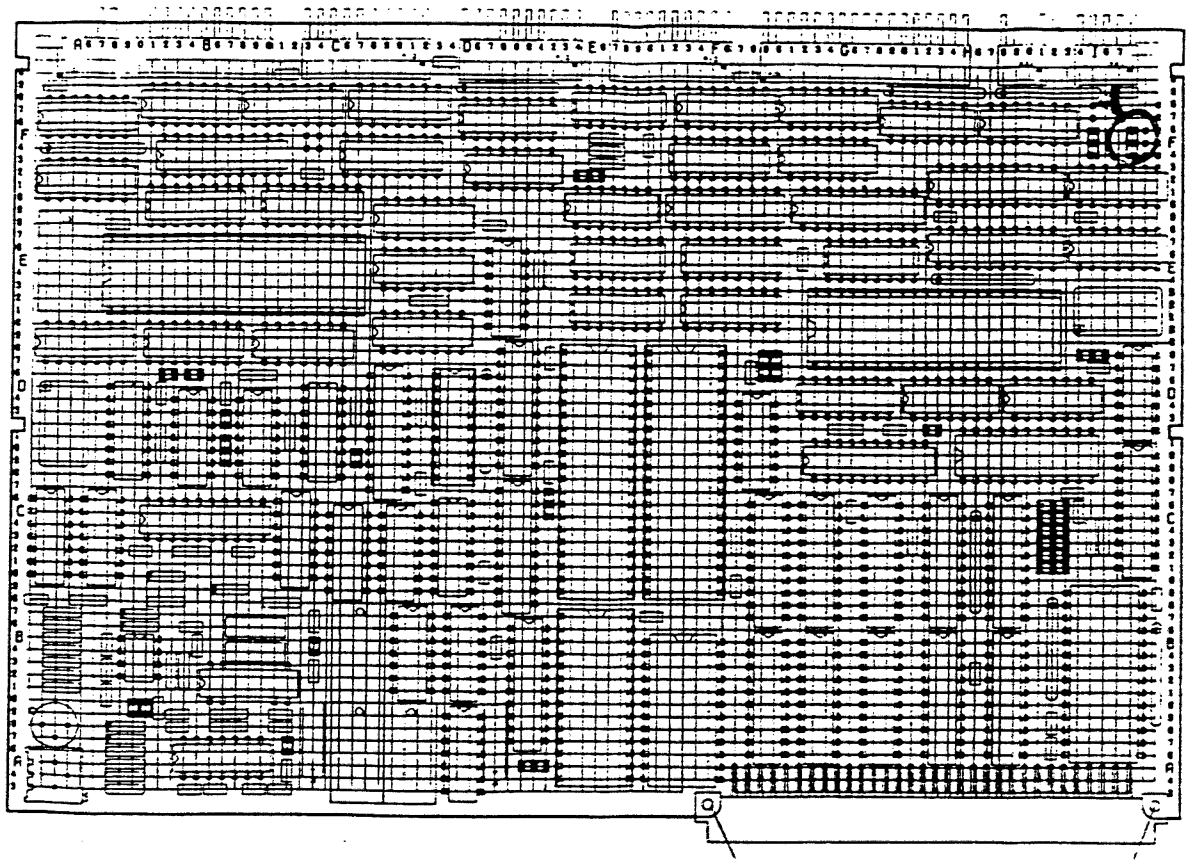


8" box strapped as drive 1



8" box strapped as drive 0





service information | FIELD CHANGE |

system series: P800 P4000 P6000 P9000
model: P829 P4200 P4202/P4402 P4502/P4802 P6923/P6924 P6966 P9200/P9300
main assy: PCB WDE1 **nr.** P829-C-016
P829-142 P4000-35 P4700-037
P6966 P6925-235
P6759-001 P6966-003
P9000-074
units affected: All
est.inst.time: 25 min.
date: 861013 **revised:**

title: Overwritten data on disk.

note: Problem nr. MSA-018-661.
this change is: Mandatory

1. CONDITION : Data inside a sector is shifted over 2 or 4 octads throughout the whole sector.
This problem shows up when the VTOC is corrupted.
For P4000 systems: during IPL a hexled code occurs like F4-10; F4-11; F4-16; F4-18; etc.

2. CORRECTION : The rising edges of the clock and signal HLDA of the DMA should not coïncide.
For WDE1 selected micro-processors will be used.

3. REMOVE : Micro-processor 8085A-2 on location F0B9 from socket.

4. ADD : Selected micro-processor witn nr. 8085A-2/00001 on location F0B9 on socket.

5. ADJUSTMENTS : None.

6. PARTS :

Description	12NC
8085A-2/00001	5122 000 19681

Order total needed amount for updating all your WDE1's before '87 from:

Philips TDS
Dept. Customer Service Material Management
Att: Mr. A. Versloot
Apeldoorn

7. STATUS CHANGE : This is Mod. 8 of the PCB WDE1.
The 12NC changes from 5122 194 48358 into 5122 194 48359.
Service 12NC: 5322 216 21586 not changed.

8. TEST FACILITIES AFFECTED : None.

9. DOCUMENTS AFFECTED : None.

10. REMARKS : None.

Responsibility: Mr. B. Berends.

STATUS CHANGE FORM

MAIN ASSY	P 829 - 142
	5122 • 194 • 48350

SUB ASSY	
	• • 0

NAM	WDE1
ID	
DK	P829-142

LEVEL	MOD	EFFECTIVE DATE	EFFECTIVE SER#	SERVICE INFO P8..	SERVICE INFO COND	SUBJECT, REMARK
1		INITIAL		29 C		
2						
3						
4	3	8510		007	M	several errors
5	4	8510		008	R	incompatible with 4000SL, never Comm=M
6	4	8511		009		BA221 replaced
7	5	8605		011	R	µpr->1 (from WDI)
	6	8609		014	R	µpr->2
8	7	8610		015	R	IPL from 8" floppy via WDE
9	8	8610 8611		016	M	Overwritten data

REPLACED BY	• •	NAM

OTHER CONCERNING SI			
829 C 018	WDE / WDI		

service information | **FIELD CHANGE** | Data Systems

system series: P800, P4000, P6000, P9000
model: P829, P4200, P4202/P4402, P4502/P4802, P6923, P9200/P9300
main assy: PCB WDE **nr.** P829-C-007, P4500-222, P6923-016, P9000-028
units affected: All
est.inst.time: 45 min.
date: 851007 **revised:**

title: WDE problems

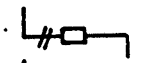
note: Previous SI P4200-023

this change is: Mandatory

1. CONDITION : - Excessive recoverable errors on track zero of the flexible disk.
   - False "Write fault" indication from the Seagate 10M fixed disks.
   - When switching power on, data sets can be overwritten if the fixed and/or flexible disks are located in an extension cabinet (P3437, P3438, P9101).

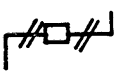
2. CORRECTION : Modify the PCB WDE.

3. REMOVE : IC 74F08 at location C5B9. This IC is removed only to facilitate the modification it is then replaced.
On componentside, cut the following printed connections:

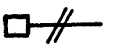
C1C6 

C8C3 

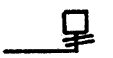
A8F3 

G4F6 

On soldering side:

C8C4 

A4D7 

A5F3 

4. ADD : IC 74F08 at location C5B9.

On soldering side, make the following connections:

D6C4 - D0B7	J0C3 - G4F6
C1E0 - C5C5	G4F6 - A8F3
C8C3 - C5E0	C9C5 - D0B6
C8C4 - D0B5	A7F5 - A5F3
A8E5 - A4D7	G6F9 - G4F3

5. ADJUSTMENTS : None.

revised: nr. P829-C-007
P4500-222
P6923-016
P9000-028

6. PARTS : Description | Service 12NC

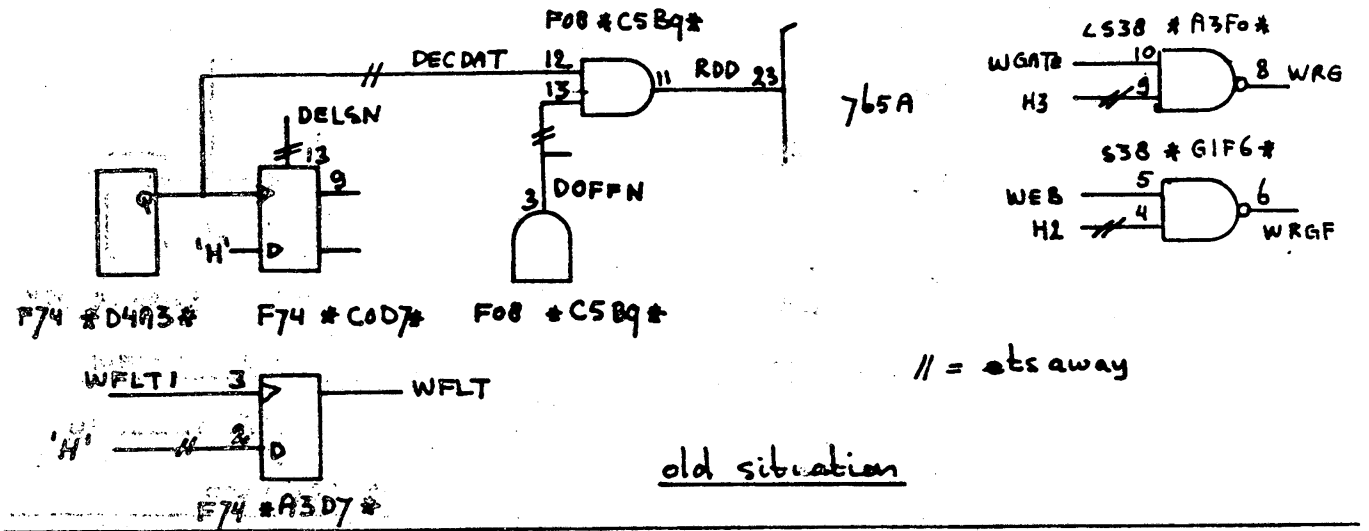
Description	Service 12NC
IC 74F08	5322 209 81574

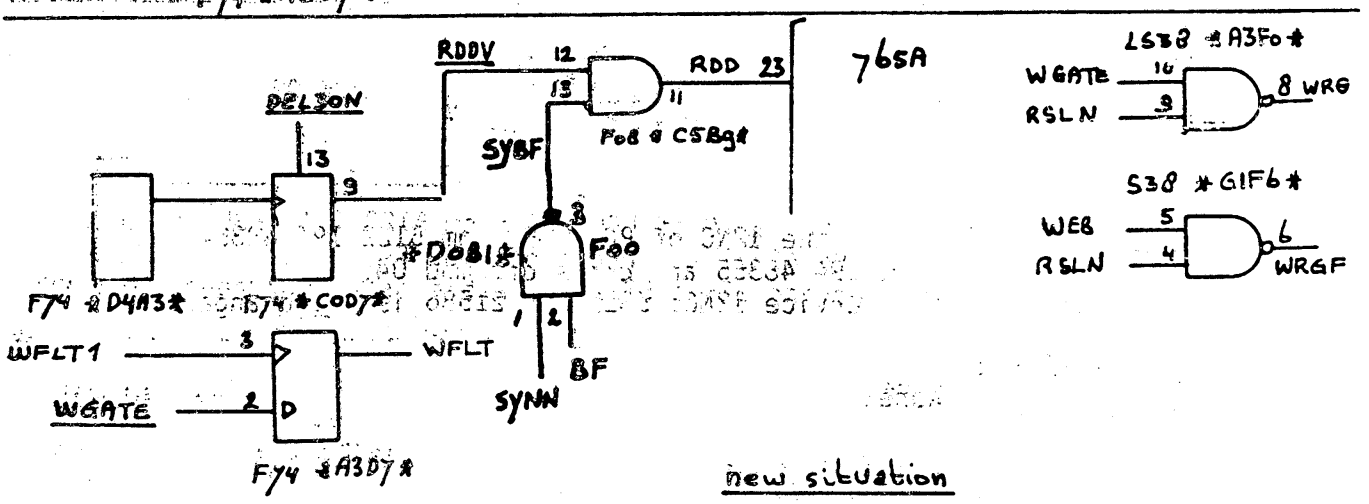
7. STATUS CHANGE : Change the 12NC of PCB WDE from 5122 194 48353 into 5122 194 48354 and cross off mod 03.
The service 12NC: 5322 216 21586 is not changed.

8. TEST FACILITIES AFFECTED : None.

9. DOCUMENTS AFFECTED : Schematics 5122 194 48350 sheet 140 pages 4, 5 and 6 (see drawing).

10. REMARKS : Previous SIs for the PCB WDE had only P4200 numbers. Now, the PCB WDE is also used in P4502/P4802 Slimline models, P800, P6000 and P9000 so, the SIs will have P800, P4500, P6000 and P9000 numbers.





service information | **FIELD CHANGE** | Data Systems

system series: P800, P4000, P6000, P9000
model: P829, P4200, P4202/P4402, P4502/P4802, P6923, P9200/P9300
main assy: PCB WDE **nr.** P829-C-008, P4500-223, P6923-017, P9000-029
units affected: All
est.inst.time:
date: 851007 **revised:**

title: WDE in P4000 Slimline.

note: Previous SI P829-C-007/P4500-222/P6923-017/P9000-029
this change is: SEE REMARKS

1. CONDITION : The PCB WDE cannot be used in P4000 Slimline. The circuit for determining the CU number is not compatible with the combination of UPL-2 Bus and P4000 HSI.

2. CORRECTION : Modify the PCB WDE so it can be used in P4000 Slimline, P4000 present line and P9000.

3. REMOVE : On soldering side cut the following printed connections:

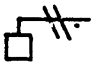
G4C5



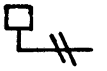
G2A4



G1A4



G0A4



On component side:

IOB6



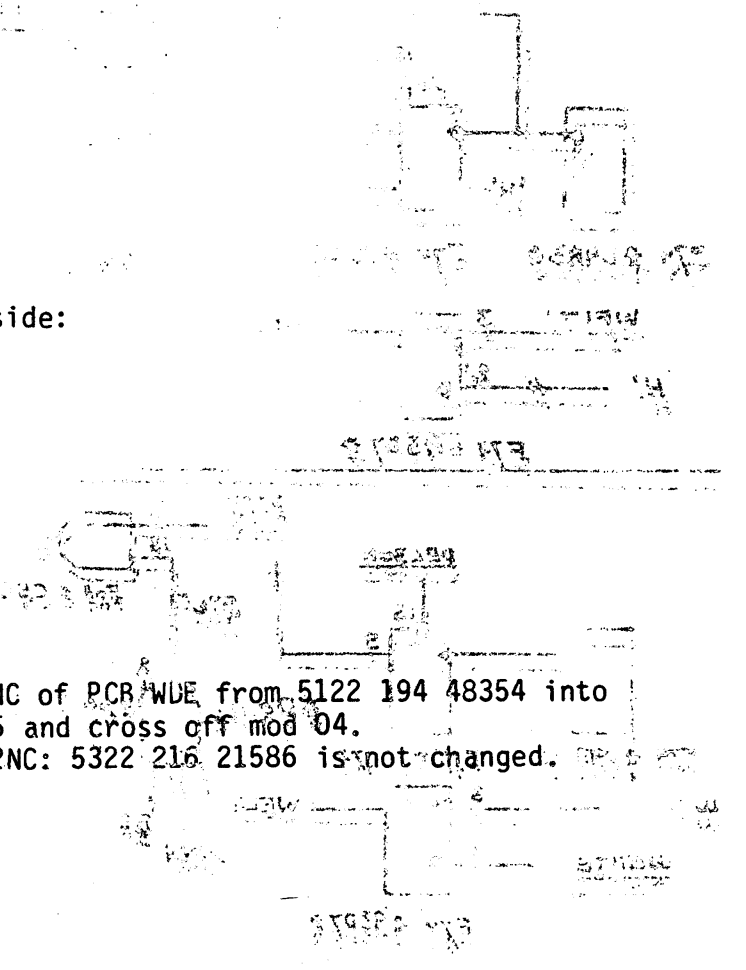
4. ADD : None.

5. ADJUSTMENTS : None.

6. PARTS : None.

7. STATUS CHANGE : Change the 12NC of PCB WDE from 5122 194 48354 into 5122 194 48355 and cross off mod 04.
The service 12NC: 5322 216 21586 is not changed.

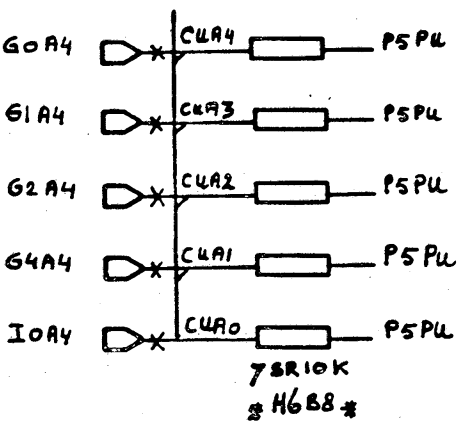
8. TEST FACILITIES AFFECTED : None.



9. DOCUMENTS AFFECTED : Schematics 5122 194 48350 sheet 140 page 2. (see drawing).

10. REMARKS : With this change, the automatic slot recognition is disabled on the WDE so, the straps must always be set for the proper CU number when using the WDE in P4000 present line, P4000 Slimline, P9000, P800 or P6000.
This change is mandatory for a WDE used in P4000 Slimline and Retrofit on failure for a WDE used in P4000 present line, P9000, P6000 and P800.

Functional diagram SH140-2



service information

| TECHNICAL TIP |

Data Systems

system series: P800	**model:** P829	**main assy:** PCB WDE	**nr.** P829-C-009
P4000	P4200		P4500-227
P6000	P4202/P4402		P6923-018
P9000	P4502/P4802		P9000-034
	P6923/P6927		
	P9200/P9300		

date: 851122 **revised:**

title: Replacement of BA221 diodes.

note:

The 12NC of the WDE is changed from 5122 194 48355 into 5122 194 48356.
The BA221 diodes at locations B5B9 and B0C0 are replaced by Hewlett Packard diodes 5082-2835.

This is not a functional change, the diodes were changed because the BA221 type had a high rejection rate (± 2%) during production and testing.

On the PCBs in the field the diodes have been tested so the 12NC can be changed from 5122 194 48355 into 5122 194 48356 without changing the diodes.
The Mod. number 04 and service 12NC: 5322 216 21586 are not changed.

Previous SI P829-C-008
P4500-223
P6923-017
P9000-029

Responsibility: Mr. E. Silva.

service information

PHILIPS

FIELD CHANGE

system series: P800, P4000, P6000, P9000
model: P829, P4200, P4202/P4402, P4502/P4802, P6923, P9200/P9300
main assy: PCB WDE1 **nr.** P829-C-011, P4700-021, P6925-223, P9000-059
units affected: All
est.inst.time: 2 hours
date: 860522 **revised:** 860827

title: Microprogram release 1 for WDE1 (new PROM 40021).

note: Previous SI P829-C-009/P4500-227/P6923-018/P9000-034
this change is: Retrofit on failure

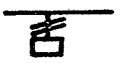
1. CONDITION : Microprogram Rel. 1 was planned to be introduced with release of WDI.
For WDE it is introduced as well, because of hard disk performance improvement by seek overlap. In practice this improvement is only noticeable when a data management system uses more than one hard disk drive.

2. CORRECTION : The microprogram size is doubled to 16kB (before = 8kB), so an additional addressline is needed (= A14). This addressline is also led to FPLA-1 and FPLA-2 for RAM selection .

3. REMOVE : On component side (see page 2)

- EPROM, type 2764-3, location E3A4.
- IC socket where EPROM is mounted on.
- FPLA-2, type 82S153, location D8C9.
- Strap test 2, location E4F2 (see page 2).

Cut the following connections:

- P5PU  E9B5 component side
- (A13)  E9A9 soldering side
- (A13)  D8A9 soldering side

4. ADD : Remount IC socket
EPROM 27128-3 at location E3A4
FPLA-2 82S153 at location D8C9

On the soldering side make the following connections:

- F1A9 - E9B5 (A13)
- F6C5 - E9A9 (A14)
- D8C1 - F6C5 (A14)
- D8D8 - D8C1 (A14)

5. ADJUSTMENTS : None.

Responsibility: Mr. B. Berends.

CO 86.0211

6. PARTS : Description | 12NC

Description	12NC
EPROM	5122 194 40021
FPLA-2	5122 194 39522

PROMs can be orderd from:

Philips TDS
Dept. Customer Service Material Management
Att. Mr. A. Versloot
Apeldoorn

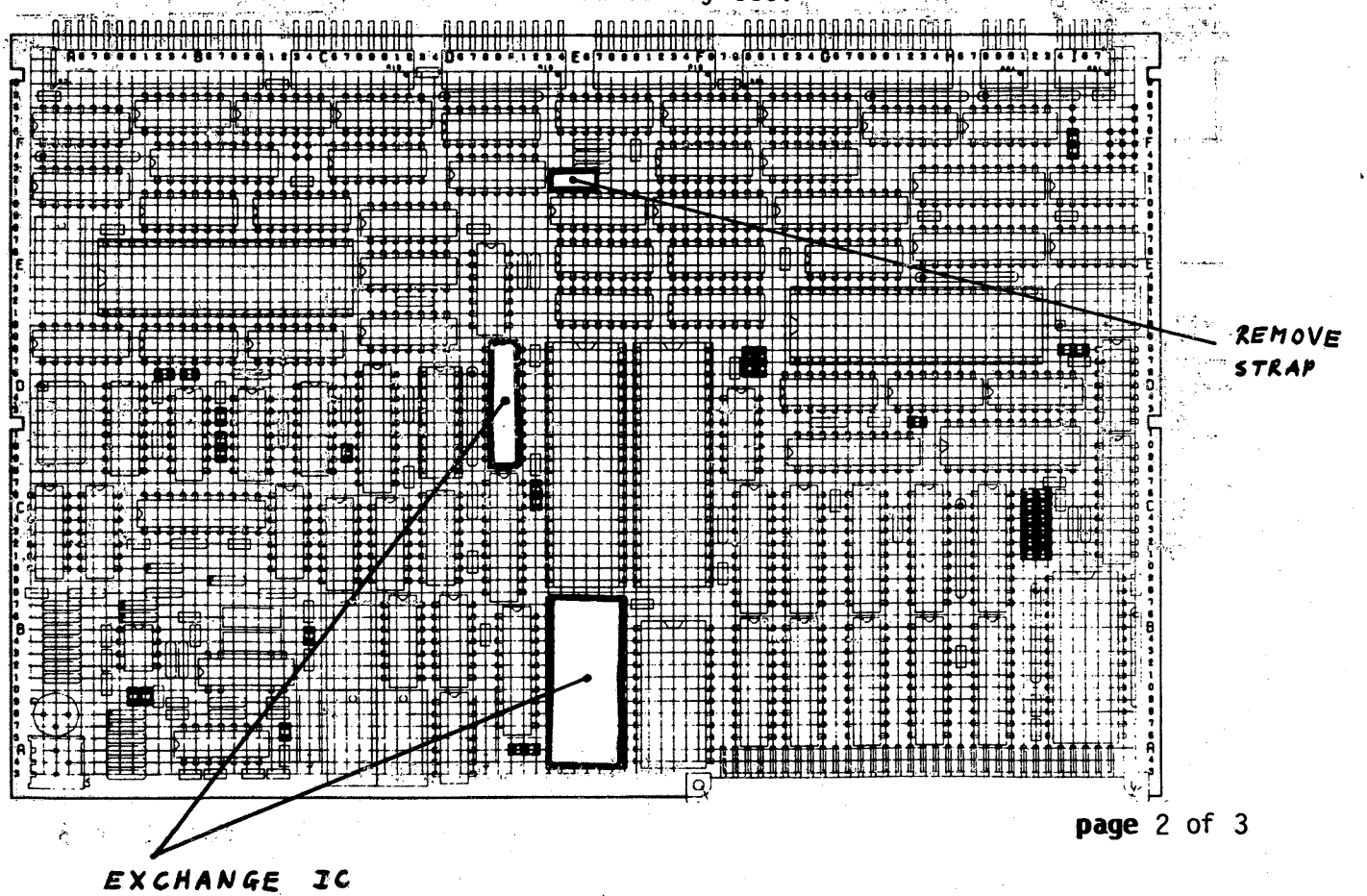
7. STATUS CHANGE : This is Mod. 5 of the PCB WDE1.
The 12NC changes from 5122 194 48356 into 5122 194 48357.
Service 12NC: 5322 216 21586 not changed.

8. TEST FACILITIES AFFECTED : None.

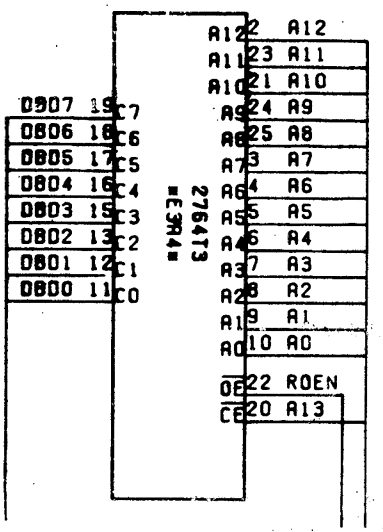
9. DOCUMENTS AFFECTED : Schematics 5122 194 48350 sheet 140 pages 3 and 5 (see page 3).

10. REMARKS : From this mod. level on additional improvement on IPL and overlay loading can be achieved by using a utility. "Program Load Improvement".

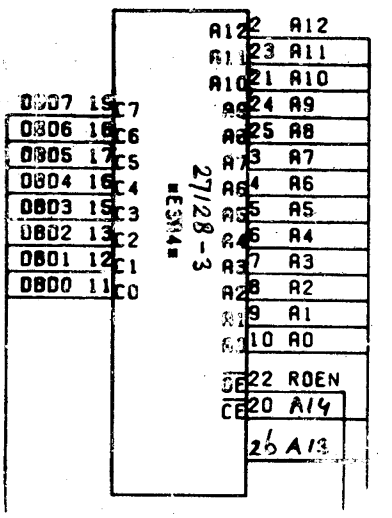
The utility will be part of the SSS tool information system and will be announced by SSS.



revised: nr. P829-C-011
P4700-021
P6925-223
P9000-059

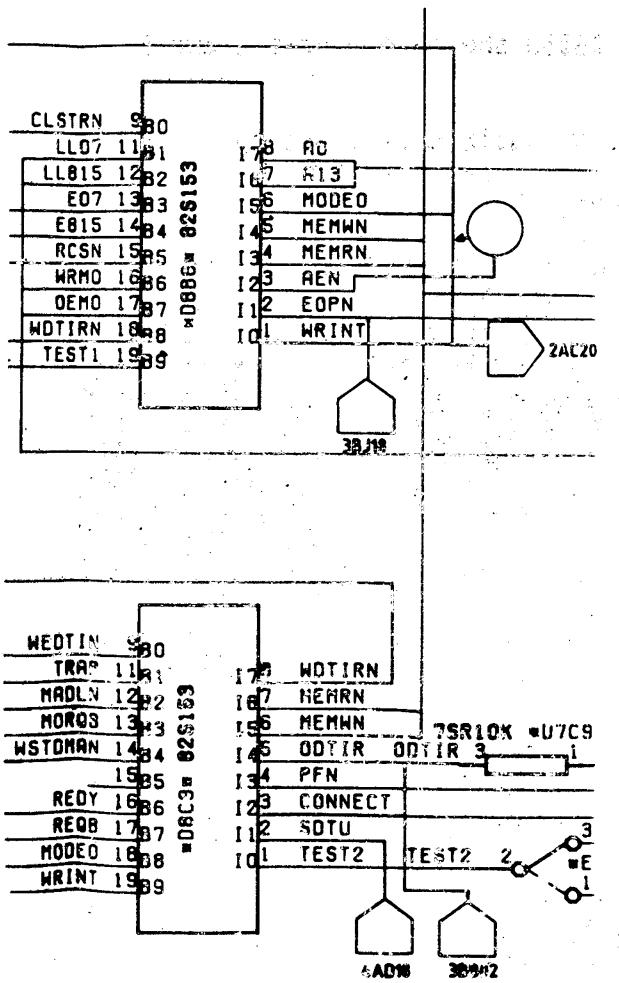


Old

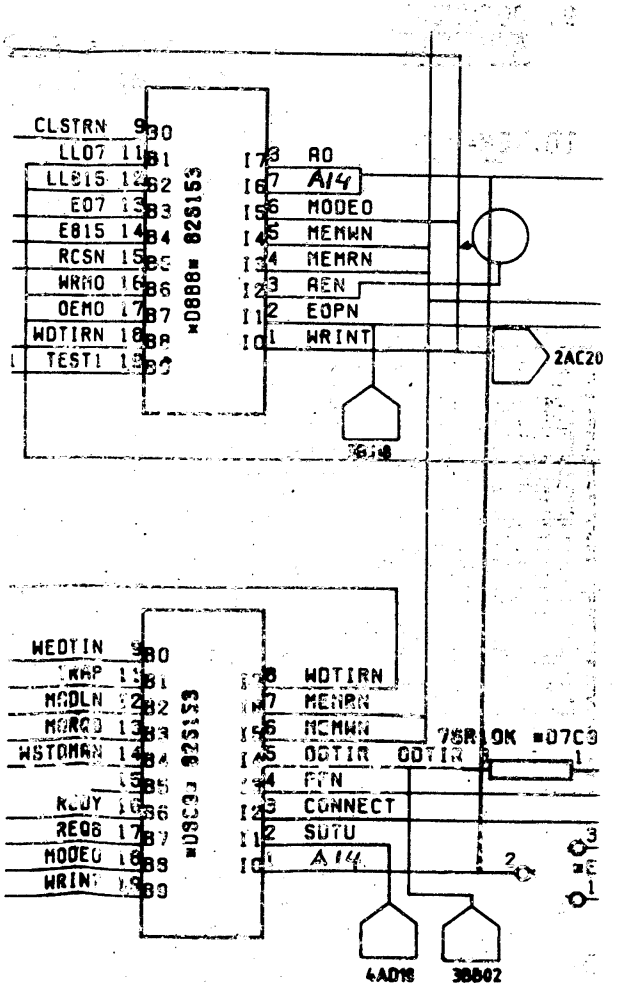


New

On schematics 5122 194 48350 sheet 140-3.



Old



New

On schematics 5122 194 48350 sheet 140-5.

service information

FIELD CHANGE

system series: P800, P4000, P6000, P9000
model: P829, P4200, P4202/P4402, P4502/P4802, P6923, P9200/P9300
main assy: PCB WDE1 **nr.** P829-C-014, P4700-035, P6925-232, P9000-072
units affected: All
est.inst.time: 10 min.
date: 860916 **revised:**

title: Microprogram release 2 for WDE1.

note: See status change.
this change is: Retrofit on failure

1. CONDITION : IPL does not work when during READ a Peripheral Attention Interrupt is received from another fixed disk connected to the same WDE.

2. CORRECTION : Exchange of microprogram.

3. REMOVE : EPROM, type 27128-3/40021, location E3A4.
(MPR identification name: 5122 194 62071).

4. ADD : EPROM type 27128-3/40022, location E3A4.
(MPR identification name: 5122 194 62072).

5. ADJUSTMENTS : None.

6. PARTS :

Description	12NC
EPROM	5122 194 40022

7. STATUS CHANGE : Mark Mod. 6 on PCB WDE1.
FActory 12NC's 5122 194 48357 is unfortunately not changed due to a mistake in the factory.
Boards which have the new EPROM Rev. level already, should be marked Mod. 6.
Service 12NC: 5322 216 21586 not changed.

8. TEST FACILITIES AFFECTED : None.

9. DOCUMENTS AFFECTED : Partslist.
Before starting this modification be shure that Mod. 5 was carried out.
(SI P829-C-011/P4700-021/P6925-223/P9000-059).

10. REMARKS : PROMs can be ordered from:

Philips TDS
Dept. Customer Service Material Management
Att. Mr. A. Versloot
Apeldoorn

Responsibility: Mr. B. Berends.

Service Information: [illegible]

Subject: [illegible] model: [illegible] [illegible]

Vs affected: [illegible] est. inst. time: [illegible]

Date: [illegible] revised:

[illegible]

Notes: [illegible] Change is [illegible]

1. [illegible] [illegible]

2. [illegible] : [illegible]

3. [illegible] [illegible]

4. [illegible] : [illegible]

5. [illegible] : [illegible]

6. [illegible] : [illegible]

7. [illegible] : [illegible]

8. [illegible] : [illegible]

9. [illegible] : [illegible]

10. [illegible] : [illegible]

Responsibility: [illegible]

[illegible]

service information | FIELD CHANGE |

system series: P800, P4000, P6000, P9000
model: P829, P4200, P4202/P4402, P4502/P4802, P6923/P6966, P9200/P9300
main assy: PCB WDE1 **nr.** P829-C-015
P829-142 P4000-35 P4700-036
P6966 P6925-234
P6759-001 P6966-002
P9000-073
units affected:
est.inst.time: 2 hours
date: 861010 **revised:**

title: IPL from 8" floppy box with WDE-1 used as control unit.

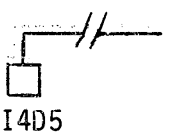
note: **this change is:** Retrofit on condition

1. CONDITION : This modification is only important if an 8" floppy box is connected.
If the 8" floppy box was adjusted as drive 0 (for IPL), an attach on drive 1 (not present) didn't return a "not operable".

2. CORRECTION : Selection is provided by means of an extra strap.

3. REMOVE : Cut track on soldering side:

- FDS1N



4. ADD : Strap at location I8F4 (on comp. side)

Jump by on soldering side:

I4D6 - I8F5 (SEL8)
G5F2 - I8F6 (FDS1V)
G2F2 - I8F4 (FDS1N)

5. ADJUSTMENTS : None.

6. PARTS :

Description	12NC	Amount	Service 12NC
Jumper 1-2P-GR	5122 000 13890	1	5322 263 60062

7. STATUS CHANGE : This is Mod. 7 of the PCB WDE1.
The 12NC changes from 5122 194 48357 into 5122 194 48358.
Service 12NC: 5322 216 21586 not changed.

8. TEST FACILITIES AFFECTED : None.

9. DOCUMENTS AFFECTED : None.

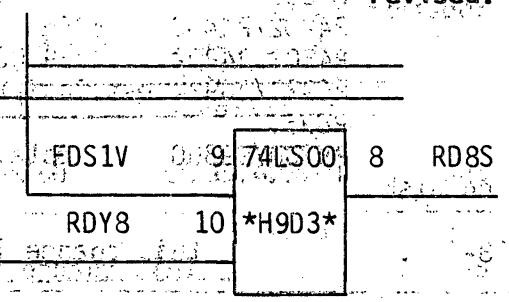
10. REMARKS :
- WDE-1 is not used as 8" floppy control unit in P6000 and P800.
- Dipswitch adjustment on drive in floppy box:
Ready 2 switch should always be closed.

Responsibility: Mr. B. Berends.

service information

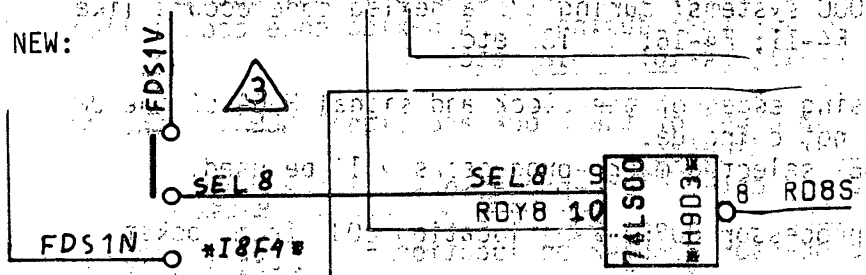
revised: nr. P829-C-015
P4700-036
P6925-234
P6966-002
P9000-061

OLD:



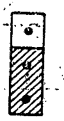
New on schematics 5122 194 48350 sheet 140-04:

NEW:

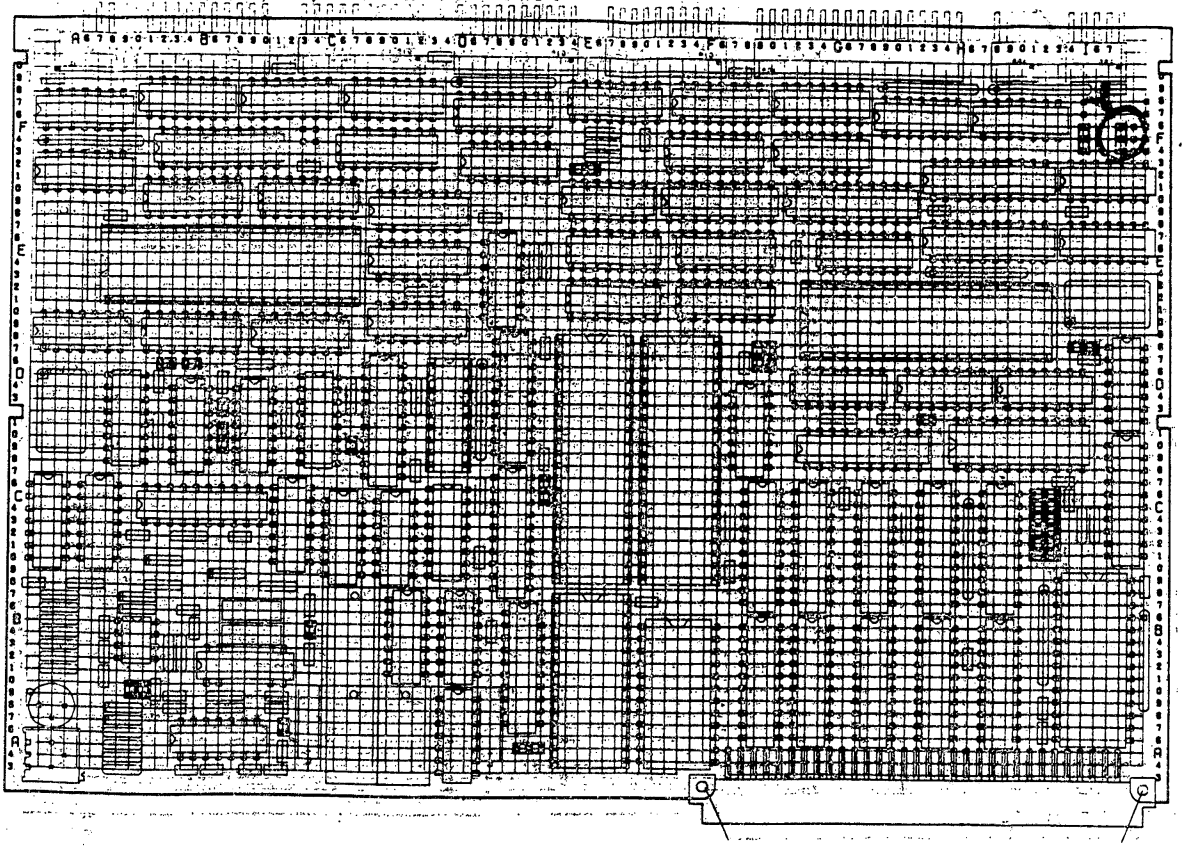




8" box strapped as drive 1



8" box strapped as drive 0



service information

FIELD CHANGE

PHILIPS

system series: P800 P4000 P6000 P9000
units affected: All

model: P829 P4200 P4202/P4402 P4502/P4802 P6923/P6924 P6966 P9200/P9300
main assy: PCB WDE1 **nr.** P829-C-016
P829-142 P4000-35 P6759-001
est.inst.time: 25 min.

P4700-037 P6925-235 P6966-003 P9000-074

date: 861013 **revised:** 861110

title: Overwritten data on disk.

note: Problem nr. MSA-018-661.

this change is: Mandatory

1. CONDITION : Data inside a sector is shifted over 2 or 4 octads throughout the whole sector.
This problem shows up when the VTOC is corrupted.
For P4000 systems: during IPL a hexled code occurs like F4-10; F4-11; F4-16; F4-18; etc.

2. CORRECTION : The rising edges of the clock and signal HLDA of the DMA should not coincide.
For WDE1 selected micro-processors will be used.

3. REMOVE : Micro-processor 8085A-2 on location F0B9 from socket.

4. ADD : Selected micro-processor with nr. 8085A-2/00001 on location F0B9 on socket.

5. ADJUSTMENTS : None.

6. PARTS :

Description	12NC	Service 12NC
8085A-2/00001	5122 000 19680	5322 209 71483

Order total needed amount for updating all your WDE1's before '87 from:

Philips IDS
Dept. Customer Service Material Management
Att: Mr. A. Versloot
Apeldoorn

7. STATUS CHANGE : This is Mod. 8 of the PCB WDE1.
The 12NC changes from 5122 194 48358 into 5122 194 48359.
Service 12NC 5322 216 21586 not changed.

8. TEST FACILITIES AFFECTED : None.

9. DOCUMENTS AFFECTED : None.

10. REMARKS : None.

Responsibility: Mr. B. Benends.

Service Information

FIELD CHANGE

[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]

service information | FIELD CHANGE |

system series:	P800	**model:** P829	**main assy:** PCB WDE1	**nr.**	P829-C-018
	P4000	P4200	P829-142 P4000-35		P4500-241
	P6000	P4202/P4402	P6966		*P4700-085
	P9000	P4502/P4802	P6759-001		P6925-243
		P6923/P6924			P6966-004
		P6966			P9000-110
		P9200/P9300	**date:** 870319	**revised:**	870917

title: WDE/WDI disk controllers used in PTS computers.
(new µprogram release WDE-1).

note:

When WDE or WDI disc controllers are used in PTS (TOSS) computers, the software requires that the controller returns the 12NC: 5122 194 5639x as a response on the "get identity" command from the software.
All WDI cards and also WDE cards from level 5 however will return a different 12NC which has made it impossible to use these cards in TOSS systems.
For this reason a new PROM 5122 194 65181 has been introduced on WDE (becomes Mod. 9).
This PROM will return the correct identity for use in TOSS systems.
This PROM also has to be used on WDI cards installed in TOSS systems.

The background of this story is explained below:

In PTS 6920 computers the WDE/WDI is used for connection of 5.25 inch Hard Disc drives.
For connection of 8 inch hard disc drives other control units are used. These can be WDC or WDH.
Because the method of addressing the drives is different for WDE/WDI as compared to WDC and WDH it is necessary for the software to know which type of controller is present.
For this reason the software (and also the IPL program) is using the command "Get identity" to identify the type of control unit.
This command will return the 12NC of the control unit microprogram to the software and so enables the identification of the controller by the software.

TOSS software up to release 15 was expecting one of the following control units: WDD, WDC, WDH or WDE.

Because WDE is the only controller in this group having a unique addressing method (first hard disc is unit 1 instead of 0), the software is checking only for presence of WDE.
In case a WDE is present the 12NC: 5122 194 5639x is returned.
If this number is recognised by the software, the WDE addressing will be used.
When WDE became end of life, it was succeeded by WDI, with a different microprogram 12NC.
This 12NC ending with 6207x is of course not recognised by the software and as a result a wrong addressing method will be used, resulting in a disc not operable status.

To make matters worse this same microprogram was also introduced on WDE from level 5.
Now the software does not recognise the WDE and WDI.

Responsibility: Bert Berends.

BB

revised: 870917 **nr.** P829-C-018
* P4500-241
* P4700-085
P6925-243
P6966-004
P9000-110

To solve this problem a new microprogram was introduced for WDE with the same 12NC as the original WDE number (5639x).
This microprogram is available in the PROM with 12NC: 5122 194 65181.

At this moment a microprogram for WDI with the original 12NC is not yet officially available.
To solve this problem in the field it is recommended to install the PROM 5122 194 65181 also on all WDI cards used in TOSS systems.

All WDI card delivered from PEAB will be modified in the factory and will get a new 12NC number 5131 196 01880.

Spare parts delivered from Concern Service (5322 216 21776) will be delivered with the official WDI-PROM (4002x) giving the ident 6207x).
Before installation in a TOSS system the PROM for these cards has to be exchanged and the PROM 65181 has to be installed.

To summarise the WDE/WDI situation:

PCB	PROM	IDENT	for use in TOSS	OTHERS
WDE		5639x	OK	OK
WDE	4002x	6207x	NOT OK	OK
WDI	4002x	6207x	NOT OK	OK
WDI	65181	56394	OK	OK

(Others = P800, P4000 and P9000).

The 12NC for WDE is 5122 194 4835x Service 12NC: Same as WDI.
The 12NC for WDI is 5122 194 6297x Service 12NC: 5322 216 21776.

Special PEAB version of WDI including PROM 65181: 5131 196 01880.
This card does not have a service 12NC, for spareparts the normal WDI should be ordered.

PROM can be ordered at:

PTDSN BV
Dept: Customer Service/Logistics.
Att. Mr. A. Lis or Mr. A. Versloot.
Apeldoorn.
Telex Route Ind: N/LAACSM